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13. ABSTRACT (Maximum 200 words) This report describes the results of a three-year research program aimed at improving the understanding of the operation of GaAs photoconductive switches that are an integral component of a high power, ultra wideband microwave generator. The research performed revealed the following results: material properties associated with the production of the GaAs wafer prior to processing are critical in determining the switches' final operating characteristics. In particular, high dc bias-initiated breakdown was demonstrated to occur not due to surface flashover, but rather to trap-filled sites in the vicinity of the electrode contacts; the inclusion of an n+ layer near the electrodes was demonstrated in simulations to mitigate the effects of high dc bias-initiated breakdown; the use of keV to MeV range electrons impacting the GaAs resulted in the formation of new defect levels as a result of nonionizing energy loss (NIEL) processes-this led to an increase in the dc hold-off of photoconductive switches; finally, a self-consistent, two-dimensional, time-dependent, drift diffusion model was developed to simulate the response of high power photoconductive switches-persistent photoconductivity was shown to arise at high bias even under the conditions of spatial uniformity; under strong uniform illumination, the spatial nonuniformities were quenched as a result of a polarization-induced collapse in the internal fields. Experimental work was performed to fabricate prototype switches to better understand the modeling work. This was met with mixed results due to the difficulties in reproducing the fabrication process developed earlier by researchers at ARL. Ongoing work is aimed at addressing this latter issue.					
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# **FINAL REPORT**

## **Optimization of GaAs Photoconductive Switch Technology for Ultra Wideband Applications**

**AFOSR New World Vistas Grant F49620-97-1-0320**

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## I. SUMMARY of WORK at UNM

Our three year research effort on studies of photoconductive semiconductor switches (PCSSs) was targeted at improving the performance of the switches used specifically in experiments generating ultra wideband (UWB) high power microwaves (HPM) at the Directed Energy Division of the Air Force Research Laboratory (AFRL), Kirtland AFB New Mexico. PCSSs made from high resistivity semi-insulating (SI) GaAs and operating in the non-linear mode are used as the main switch in a setup for microwave generation. Two of the limiting factors in the operation of these microwave generators, from the PCSS's perspective, have been the inability of the switches to operate at bias greater than 20-30 kV, and their failure after a certain number of shots or switching operations.

Our initial studies of the PCSS were focused on premature breakdown mechanisms of the opposed contact devices used in generating UWB HPM. This study was important since the theoretical breakdown of the device material is an order of magnitude greater than the operating values, and also because lower bias operations limit the risetime and the subsequent energy transferred to the load, which is an important parameter in the operation of these switches. Thus, our study has been geared towards understanding the conduction process of the PCSS during the charging and discharging states, and their relationship to the failure mechanisms itself.

A basic understanding of the importance of traps and conduction processes in trap-dominated materials has emerged and have contributed towards our prediction as to how the switches breakdown prematurely. We have also suggested mechanisms to increase the operating voltages through better fabrication processes. We have also addressed the process of persistent conductivity and surface effects during device operation. Since deep level traps play a greater role in the conduction processes than thought earlier, any change in the trap energy level or the capture parameters (cross-section, concentration) brought about through nuclear interactions (e.g. during space based applications) may affect the device performance. Also, our research effort has brought about a better understanding of the physics of carrier transport in high resistivity materials and our analysis has shown that, even though these PCSS are of very high resistivity, the compensation process and the presence of a high level of traps make it behave more as a lifetime-type material than the well known high resistivity relaxation-type material. Besides simulation analysis at UNM and ODU, UNM has been involved in the fabrication of some of the switches for the AFRL experiments. The following Section details our research effort for the final year, which includes a report on the device processing and the process recipe for the PCSS fabrication at UNM.

## II. SIMULATION AND FABRICATION OF THE PCSS AT UNM

The PCSS studied is the same as reported in the first two years of the reporting period. The PCSS is a high resistivity material, dominated by EL2 traps near the mid-gap, and compensated by carbon. It is of the "opposed" contact type, where the contacts are made from layered refractory materials (Pd/Ge/Ti/Pt of thickness 200/400/400/300 Å, respectively). The contacts have a Rogowski profile on the front and back of the wafer, about 0.25 cm apart. The opposed contact PCSS and an AFRL schematic for generating ultra wideband high power microwaves is shown in Figure 2, Appendix E. All the current simulation studies are for PCSSs with dimensions 2.0 cm by 1.3 cm with a thickness of 0.063 cm, and it is expected that the contact length will be reduced in the new generation of PCSSs. The switch material is LEC grown, highly resistive ( $2.5 \times 10^7 \Omega\text{-cm}$ ) SI GaAs made through the compensation of a deep donor and a shallow acceptor or DDSA, as shown in Figure 1, Appendix E. Carbon is the shallow acceptor while the deep level EL2 sites act as the deep donor. The introduction of an energy level in the mid-gap is thus likely to influence the electron-hole generation, recombination, and the carrier lifetime. These effects will be seen both at the charging (off) state and the conduction (on) state of the switch. Thus, during the charging state, the hold-off voltage is likely to be affected, and during the conducting state the parameter most likely to be affected is the rise time of the switch. A summary of the research accomplishments follows in the subsequent sections of this report, first with the simulation details and fabrication effort at UNM.

## II\_A THE SIMULATION MESH

Simulation studies in the first two years have indicated that the physical conditions at the vicinity of the contacts have a greater influence on the PCSSs' performance than in the bulk of the material. Thus the mesh has been refined accordingly, with a large separation between the mesh points in the bulk and a fine separation near the contacts. This gives a better electric field, trap density and other important parameters' profiles for analysis. The current mesh, however, still has the limitations of the previous meshes in terms of the device geometry and contact materials. The mesh for the opposed contact still has an active region (the distance between the contacts) separation of 0.25 cm, which is the same as in the actual device. This is important as it may help in preserving the device physics both during conduction and the charging state of the switch. This is a marked improvement over earlier simulations where the mesh generated was about 1/40 of the original device size, which also included the distance between the active regions. This was done primarily due to the limitations of computing speed, memory requirements of the computational tools, and the available software modules. The contact length for all the simulations is still 100  $\mu\text{m}$  as opposed to the original length of about 0.875 cm. Also, like most simulations in the first two years, only the material that is in intimate contact with the device (Pd) has been defined as the contact material for the simulations. We do not anticipate that this approximation will in any way affect the results since the first contact material (e.g. its properties, such as work function) will determine carrier injections, etc., and will represent all the physics associated with the device's conduction process. This has the added advantage of drastically reducing the simulation time. In the next phase of our work we expect to study the the new generation of PCSSs now being used at the AFRL that has a contact length that is much smaller than 0.875 cm.

### II\_A.1 SIMULATION CODE

As in the previous years, simulations were carried out using the SILVACO software. This is a comprehensive tool that can perform semiconductor process, device, and circuit simulations using a common interface. Thus a device can be "virtually fabricated" using the ATHENA module and then can be a part of a circuit where the response of the circuit to changing device parameters can be analyzed. The code includes numerous models and parameters that can be defined for any specific situation to obtain the best results possible. The code, with a main interface (ATLAS) and other interactive tools, provides for a 2- and 3-D semiconductor device simulation that also includes thin film transistors (TFT), quantum devices, heterostructures, and power devices. In addition to the drift-diffusion model, one can study such "non-local" effects as velocity overshoot, reduced energy-dependent impact ionization, *etc.* using the energy balance model wherein such transport parameters as mobility and impact ionization become functions of the local carrier temperature rather than the local electric field. A new SMARTSPICE circuit simulation module has been added to the simulation suite. The circuit simulation module includes loss and lossy transmission line elements, all known device models, polynomial capacitors, temperature-dependent resistors and capacitors and a variety of voltage and current sources. Circuit simulations can be configured for DC, AC, transient, and frequency-noise analysis. Finally, the code also has a provision to incorporate user-defined functions through a C-interpreter. This interpreter can be used in a variety of ways, such as changes in carrier mobilities, generation rate, etc. The simulation provides a self-consistent solution of Poisson's equation and the continuity equation, describing the variation in electrostatic potential with local charge densities. The evolution of electron and hole densities due to transport, generation, recombination, *etc.*, can be later plotted for analysis.

As noted earlier, the code provides for the generation of carriers throughout the device, or at a particular node. This is accomplished through the C-interpreter function addressed through a pointer in the input file. The user can implement a generation function, which may change in intensity at a distance from the source. The effects are similar to radiation induced carrier generation that we have studied for some time. Thus a number of phenomena such as latchup, CMOS burnout as a result of carrier generation due to microwave sources can be studied with the device module of the TCAD suite.

Furthermore, bulk heating of the device can be analyzed through absorption of radiation with associated changes in permittivity. The simulation device can then be divided into a number of regions with each region with a given permittivity value. In the absence of a (microwave) radiation source these values do not change. Following interaction with the source, microwave heating of dielectric will occur and surfaces

interacting with incoming radiation may have a different permittivity value than other regions of the device. The resulting field, carrier concentration, and voltages as a result of this change can be extracted through simulation and analyzed in terms of the overall behavior of the device under microwave radiation.

Besides changes in permittivity, the heating of the contacts/interlinks due to any known process also results in a number of heat sources that may affect the device's performance. The GIGA module accounts for lattice heat flow and general thermal environment through the incorporation of Wachutka's thermodynamically rigorous model of lattice heating that includes Joule heating, heating and cooling due to carrier generation and recombination, and the Peltier and Thomson effects. The dependence of material and transport parameters on lattice temperature and thermal environment is also included in the module. Thus bipolar, MOS, IGBT, thyristors and electrostatic discharge (ESD) protection devices can be studied with the module.

Introduction of new modules have greatly enhanced the simulation capabilities at UNM. The results of our simulation studies as summarized earlier, have been presented and published in such forums as International Conference on Plasma Science (ICOPS), Pulsed Power Conference, Nuclear and Space Radiation Effects Conference (NSREC), Journal of Applied Physics, EUROEM and its accompanying book *Ultra Wideband Short-pulse Electromagnetics*.

## II\_B .DEVICE FABRICATION

A number of PCSSs fabricated at the Center for High Tech Material (CHTM) facility of UNM were handed over to the AFRL, Kirtland AFB for testing. Prior to this testing under actual experimental conditions which required the switch voltages to go as high as 20 kV, the PCSSs were tested for contact integrity at lower voltages. The maximum allowable voltage for testing the contact integrity was 1 kV. These tests were conducted at the Space Vehicles Division of AFRL at Kirtland AFB, New Mexico. Currently we are working on building a tester at UNM in close coordination with the Directed Energy Group, AFRL and NSWC. All necessary parts have been ordered the work has been assigned as a student summer project. As reported earlier, most of the switches fabricated, except for one, did not do well in the experiments. It was therefore decided, in consultation with the AFRL DE Division, that the fabrication process at UNM will be normalized to that of the NSWC process. However due to equipment, deposition scheme constraints it is not possible to duplicate the NSWC process in its entirety. The discrepancies in the two processes are listed in the report shown in APPENDIX A. Even though some of the fabrication processes included pattern development, nitride deposition, baking, etc., are similar, metal evaporation and anneal temperatures are different and need further study. Other problems encountered included surface cleanliness and contamination, silicon nitride quality (generally poor), equipment failure during a critical process (metal evaporator), and scheduling (the equipment gets a lot of use and equipment downtime was often extensive).

Our effort during the final year was geared towards fabrication of the base switches and emphases on the development of the next generation of switches were scaled down until the processes are perfected. Repeatability of the fabrication processes and increase in the yield is the basis for future PCSS fabrication studies.

Baseline and prototype PCSS devices were fabricated at CHTM based on the devices modeled by the Electrical and Computer Engineering (EECS) department at UNM. The baseline device was made from both liquid encapsulated Czochralski (LEC) grown, semi-insulating GaAs and vertical gradient freeze (VGF) material. The bulk material specifications are given in APPENDIX E. The switch dimensions are 2.0 cm by 1.3 cm with a thickness of 0.063 cm. The metallization scheme used for the refractory ohmic contacts is given in APPENDIX A. The contacts have a shape based on a Rogowski profile. The Rogowski pattern increases switch lifetime by producing uniform fields between the contacts and is thought to promote random filamentation. The surface area of the device not covered by a contact is protected by a 1000 to 1500 angstrom layer of silicon nitride ( $\text{Si}_3\text{N}_4$ ). This nitride acts as both a passivation and encapsulating layer. Passivation is needed to prevent the occurrence of surface charge. An encapsulating layer is needed to prevent the possible outgassing of arsenic during processing. GaAs decomposes to evolve arsenic vapor if heated above 480 °C. Another reason for an encapsulating layer is to prevent the possible removal of EL2 centers near the surface during a high temperature hydrogen anneal.

Because of fabrication constraints, the finished prototype device is different from the model reference. The model calls for an  $n^+$  doped layer of 15 to 20  $\mu\text{m}$  below the surface underneath the negative electrode. The options for obtaining this region are (1) Diffusion, (2) Ion implantation, and (3) Epitaxial growth. Both diffusion and ion implantation were deemed infeasible for creating an  $n^+$  region with a depth of 15 to 20  $\mu\text{m}$ . For this reason, it was decided to create an  $n^+$  step by growing a doped layer above the sample surface followed by patterning and etching to remove the unwanted  $n^+$  material. Because of the availability of MBE machines at CHTM, this  $n^+$  GaAs layer was grown with an MBE. I-V testing was done on the test devices (both LEC and VGF) so that a comparison of the I-V characteristics could be made between the prototype and baseline. A case can be made that the prototype device shows an improvement in hold-off voltage if the prototype device shows lower leakage current than the baseline device for a given bias. These devices were tested up to 1000 V.

Each device was tested at 200 V, 400 V, 600 V, 800 V, and 1000 V. The voltage source was connected to one terminal of the device and the other terminal was connected to the system ground. The device was then pulsed, after which there was a three-minute waiting period to ensure that the device would not be saturated before the next measurement.

High voltage ( $> 5$  kV) testing was performed on a limited number of test devices (both LEC and VGF) to determine (1) the maximum hold-off voltage, and (2) if the device achieved lock-on. A pulsed voltage is applied to the switch which was then triggered using a compact, high-power pulsed laser diode. The baseline devices start to diverge from the prototype device at approximately 600 V. The baseline curves shift upwards while the prototype curves (forward biased) remain below the baseline curves. This follows the model prediction.<sup>2</sup>

During the high voltage testing ( $> 1$  kV) the LEC baseline device was able to hold off a voltage of 16 kV. This switch achieved lock-on mode and had a lifetime of 500 shots. The LEC prototype device was only able to hold off a voltage of 7.5 kV. This was not a high enough voltage to achieve lock-on mode.

The VGF devices fared less well. The VGF baseline device reached a voltage of approximately 12 kV but was unable to maintain this voltage and failed. The VGF prototype device reached a voltage of 5 kV before it too failed. The voltage plot for this device was not available.

The fabrication processes involved in creating an  $n^+$  region for the prototype device may result in creating surface states or traps. At lower electric fields, these additional traps act as recombination centers, which reduce the number of excess carriers which leads to lower leakage currents. This explains the I-V characteristics at lower biases.

As the electric field across the device increases, de-trapping occurs which results in an increase in excess carriers. De-trapping is even more pronounced near the surface where electric fields can achieve higher values due to surface irregularities. This electric field crowding can lead to significantly lower breakdown voltages due to unstable filamentation and charge accumulation. The following sections describe how the fabrication of the  $n^+$  region in the prototype device could result in lower hold off voltages.

## **II\_B.1 Electron Beam Metal Evaporation**

Studies have shown electrically active defects introduced during e-beam evaporation of Pt/n-GaAs Schottky barrier diodes (SBDs) have lead to significant barrier lowering. These defects are thought to be caused by stray electrons originating at the filament during metal deposition. Deep level transient spectroscopy (DLTS) measurements have confirmed the presence of defects with discrete and continuously distributed energy levels near the metal-GaAs interface. The concentration of these defects was found to increase with increasing exposure to stray electrons during deposition.

More importantly, it was found that the larger the free carrier density of the epilayer, the larger the degrading effect of the stray electrons. This can be seen in which shows that the formation of electrically active defects is linked to the dopant atoms in the GaAs crystal.

An increase in traps near the metal - GaAs interface could explain the lower I-V characteristics. These

characteristics are similar to those shown in reference 3 which shows a lower I-V curve for a baseline device after irradiation with 4 MeV electrons. In spite of an increased number of surface traps due to the irradiation this curve shows a substantial reduction in de-trapping at much lower electric fields.

## **II\_B.2 $n^+$ Step Effects**

The  $n^+$  / SI junction of the prototype device can be analyzed as a parallel-plane (semi-infinite), abrupt junction diode in which the doping concentration on one side of the junction is very large when compared with the other side.

If the edge of the junction is cut so that the area of the junction increases when proceeding from the highly doped side towards the lightly doped side, the termination is called a negative bevel junction. The establishment of charge balance on the opposite sides of the junction causes the depletion layer at the surface of the lightly doped side to decrease while the depletion layer on the heavily doped side expands. If the diffused side of the junction is heavily doped, the depletion layer shrinkage on the slightly doped side will have the dominant influence. Since the bias across the junction is being supported across a narrower depletion layer at the surface than in the bulk, the electric fields at the surface can be expected to be higher than the field in the bulk material.

In addition to this, any surface irregularities in the step such as deep furrows could result in extreme electric field crowding. Consequently, surface breakdown will precede bulk breakdown in the  $n^+$  step area.

## **II\_B.3 Effects of Wet Etching**

Although the  $H_3PO_4$  solution used to etch the  $n^+$  region is considered a polishing etch, studies have shown that the different etch rate between Ga (111) and the other planes with  $H_3PO_4$  solution lead to a severely undulated GaAs surface whose rms roughness varied by 4.6 nm in 10 min-treated samples. The  $H_3PO_4$  treated GaAs surface showed the elongated hollows and hills in one direction. The hill region was mainly composed of Ga (1 1 1) facets arrayed in the  $[-1\ 1\ 0]$  direction and contained a little more Ga than the valley. This rougher surface could adversely effect the contact quality at the anode. Remember that the epi-layer at the negative electrode region was not etched.

In addition to this, studies have shown that one sided abrupt (1 1 1) GaAs junctions have lower breakdown voltages than (1 0 0) GaAs junctions. Since the region underneath the ohmic contact at the anode is highly doped with Ge, the (1 1 1) facets resulting from the etch may have an additional detrimental effect on contact quality.

## **Conclusions**

It is possible that the detrimental effects associated with fabricating the prototype device as discussed in the previous section could override the benefits associated with adding an  $n^+$  region beneath the cathode. This is not to say the prototype design is faulty. More testing needs to be done to determine the best fabrication method for making these prototype devices.

## **III. WORK AT ODU**

### **Semi-Insulating GaAs Photoconductive Switches** (Numerical Simulations for High Voltage)

Tasks Accomplished and Work Carried Out:

#### **III.A Electrical Transport Calculations**



An appropriate mathematical model for the high-resistivity, GaAs photoconductive switch was first constructed. It was based on the assumption that GaAs can be well characterized by single conduction and valance bands within the effective mass approximation. Treatment of bulk transport within the semiconductor material was based on the Drift Diffusion approach.

A two-dimensional (2D), time-dependent numerical code was then developed to implement the drift-diffusion transport model. The salient features of this code were : (i) It was based on the drift-diffusion approach. (ii) It explicitly solved for the space- and temporal distributions of the internal electric fields and carrier densities. (iii) It yielded both the transient analysis and the steady-state response. (iv) The model was bipolar in nature, and could treat both electron and hole transport. (v) Time dependent photogeneration with a spatial profile was incorporated. (vi) Rate equations which described the transient dynamics of the free-carrier generation, trapping and recombination, were used to update carrier densities. (vii) A simple external circuit in terms of a 50 Ohm series resistance was incorporated in the model. (viii) The model took account of the internal displacement current. (ix) The numerical implementation included the possibility of carrier generation through emission from partially filled energy states within the bandgap. (x) Bulk impact ionization, and contact injection due to thermionic emission and the electron tunneling processes were taken into account. The tunneling currents were calculated based on the Wentzel-Kramers-Brillouin (WKB) approximation within the effective mass theory. A triangular potential barrier was assumed.

The two-dimensional numerical code was tested and debugged. It was then applied to evaluate and predict the DC current-voltage (I-V) characteristics of the SI GaAs switch.

The predictions compared very well with the low field DC current-voltage (I-V) characteristics available from experimental measurements at the Naval Surface Warfare Center (Dahlgren). Subsequent activity involved the application of the model for predictions of the SI GaAs switch characteristics under various conditions. These included the transient response, the DC I-V curves, and the photocurrent behavior.

The studies focussed on the role of the following processes that potentially have a de-stabilizing effect under high-field operating conditions. (A) Geometric effects at the contacts leading to non-uniformities in the electric fields, (B) Carrier tunneling at the contacts, (C) The role of barrier height fluctuations, and (D) Spatial non-uniformities in the bulk field distribution caused by space charge effects. This typically, would be due to electron-hole separation under high fields and large excitation intensities. In support of these considerations, the following types of simulations were carried out. (I) DC current-voltage curves were generated for different settings of the contact geometry. In particular, the two contact settings were assumed to vary from a geometry which yielded complete coverage of the two opposite sides, to a diagonal placement yielding only a partial coverage of each side. (II) Next, calculations of the transient photoresponse were carried out for various values of the applied bias and internal recombination time constants. The voltage values used, however, were restricted to 10 kV and were substantially lower than the predicted voltage breakdown limit of the device. (III) Finally, the role of tunneling and barrier height fluctuations was probed by imposing substantially higher voltage values on the Si GaAs photoconductor.

### III\_A.1 Thermal Calculations for the PCSS

Simulations were performed to determine the internal temperature profiles and peak temperatures of high-power SI-GaAs photoconductive switches. Almost all previous studies on the PCSS have focused on carrier transport alone. Thermal aspects, and evaluations of a potential link between failure and the large power dissipation within localized filaments have not been examined. In this study, both the transient and steady-state thermal behavior of the PCSS was probed under filamentary conditions. The approach was based on a time-domain, finite difference implementation of the heat diffusion equation taking account of the temperature dependent thermal conductivity.

The internal device temperature was obtained by solving the diffusive heat flow equation for assumed heat generation profiles. This heat flow equation contains a source term to account for the internal

power dissipation within the simulation volume. In cylindrical coordinates, the requisite equation for the thermal problem is given as :

$$\nabla \cdot \{kT \nabla T\} + g = \Delta C_p MT/Mt \quad , \quad (1)$$

where T is the temperature, g the heat generation function, k the temperature dependent thermal conductivity,  $\rho$  the GaAs density, and  $C_p$  the heat capacity. This equation can be written explicitly as :

$$\begin{aligned} & (1/r) M[kr(MT\{r,2,z,t\}/Mr)]/Mr + (1/r^2) M[k(MT\{r,2,z,t\}/M2)]/M2 + \\ & + M[k(MT\{r,2,z,t\}/Mz)]/Mz + g\{r,2,z,t\} = \Delta C_p MT\{r,2,z,t\}/Mt \quad . \quad (2) \end{aligned}$$

Due to the temperature dependent conductivity, the above equation is non-linear, and so does not lend itself to analytical solutions. Often the non-linearity is ignored by assuming  $dk[T]/dT = 0$ . Here, a temperature dependent thermal conductivity  $k(T)$  was explicitly taken. For the 300-800 K range [1-3], the parameter  $k(T)$  for SI-GaAs was approximated by as :  $k(T) = 76 - 0.1 T \text{ Wm}^{-1}\text{K}^{-1}$ . Thus, at room temperature a  $46 \text{ Wm}^{-1}\text{K}^{-1}$  value was predicted by the above expression. The governing differential equation (2) was solved using a finite difference method. Leibman's implicit formula [4] was used, since it has been shown to yield a stable solution independent of the time-step relative to the thermal time constant. Temperatures for the transient studies were obtained based on the Crank-Nicholson technique [5]. Isothermal conditions were assumed at all boundary surfaces, and their temperatures were set to the ambient value  $T_0$ . This effectively assumes that the GaAs system is capable of removing excess heat through radiation and convective processes. Equivalently, the assumed Dirichlet boundary conditions imply that the surfaces are sufficiently far away from the internal hot spots, and hence can be regarded as being in near-equilibrium with the ambient.

Our choice of the present method was based on considerations of computational ease and flexibility. For example, the finite element technique is complicated and cumbersome [6, 7], and is not needed for the relatively simple cylindrical geometry of the present problem. The transmission line matrix (TLM) for heat flow analysis has utility primarily in the time domain and for complex geometries [8, 9]. Since analysis over relatively long time scales is the present objective, use of the TLM would be inefficient. Finally, SPICE based circuit calculations based on the equivalence between thermal and the electrical systems [10, 11] require a large number of nodes, are not as transparent, and represent a "lumped-element" representation which are inappropriate for modeling high-frequency/ultrashort events.

### III\_A.2 Numerical Results Obtained

Simulation results were obtained for the device current in response to an input voltage ramp. The details are discussed in the Journal of Applied Physics paper (Ref. 12) attached in the appendix. Basically, the bias was taken to be ramped with a 1.0 ns rise time. Beyond 1.0 ns, the voltage was held fixed to four bias values of 0.1 V, 1.0 V, 10.0 V, and 100 Volts. Since the high field response can get quite complicated due to contact injection, impact ionization and tunneling effects, the low voltage regime was chosen as a simple test.

The corresponding device current predictions were obtained from the numerical model. The peak values of the currents are predicted to be about 0.001 A, 0.01 A and 0.1 Amperes, for the 1.0 V, 10.0 V, and 100.0 Volt biases, respectively. The corresponding steady state values obtained were:  $7.6 \times 10^{-9}$  A,  $8.4 \times 10^{-8}$  A, and  $8.6 \times 10^{-6}$  A. These values are in very good agreement with available experimental data and provided validation for the numerical model.

The transient curves were used to yield the final DC I-V characteristics by carrying out simulation runs over long times. The curves thus obtained were nearly linear for voltages ranging up to about 2 kV. Beyond 2 kV, a slight sub-linear behavior was predicted and associated with the negative differential characteristics of the

electron velocity-field curve. Finally, beyond about 65 kV, a dramatic increase in current is predicted. This would be due to complete trap filling and the onset of double injection. Hence, basically the SI-GaAs device under study here would effectively tend to have a hold-off voltage of about 65 kV.

### **III\_A.3 Geometric Effects on DC I-V Characteristics**

The role of the contact geometry on the DC I-V characteristics was probed by varying their size. The contacts were assumed to be on the two opposite faces, placed diagonally across each other. In the simplest configuration the two contacts fully covered each of the two opposite sides. The threshold breakdown bias is predicted to be slightly in excess of 70 kV. As before, details are discussed in the Ref. 12 attached in the appendix. Next, each of the contacts was assumed to cover half of the semiconductor area. As a result of the diagonal placement, the bottom of the first contact was in line with the top of the other, yielding minimal overlap. The I-V characteristics revealed that a much larger voltage threshold of about 100 kV is predicted. Crudely, this can be understood in terms of the increased device resistance. The effective "length" or "traversal path" for mobile carriers between the two contacts is larger for this geometry. This would lead to lower currents for a given applied voltage. Conversely, the breakdown voltage is increased for a given maximum current limit. Finally, the DC I-V predictions when each contact covered about 39 percent of the area were obtained. There was no direct overlap between the two contacts. This increased the hold-off voltage even higher. This suggests that placing contacts diagonally with relatively small areas would favorably impact the hold-off capability, and increase it well beyond 100 kV. It is expected that surface flashover effects, though not included here, would also be reduced due to the increase in contact separation for the small area geometry.

### **III\_A.4 Photocurrent Calculations for Pulsed Laser Excitation**

The transient current response to a photoexcitation pulse for a given applied biasing was simulated for different conditions. The applied bias was assumed to be a step function with a sub-nanosecond risetime. Variation of the photocurrent with time at applied voltages of 2 kV, 5 kV and 10 kV were obtained for different values of the internal recombination parameter. The laser pulse width was chosen to be 1 ns. Since the voltages were chosen to be substantially less than the threshold limit for carrier avalanche and tunneling, the photocurrent was found to decay upon termination of the laser. This is in agreement with expected behavior. Furthermore, smaller lifetimes lead to quicker decays and smaller photocurrent values.

Simulations were also carried out for a longer 10 ns laser excitation pulse. The results for the 2 kV, 5kV and 10 kV biasing voltages were similar. However, the interesting point is that during the photoexcitation process, the photocurrent was predicted to increase for material having a slower trapping time constant. With faster carrier removal as a result of a smaller lifetime, the current reached a saturating value during the photoexcitation process. This implies that the internal electric fields and space charge effects would tend to have a limiting value for a low lifetime material. This is in keeping with the conclusions reached by some researchers in the past from their experimental measurements of neutron-irradiated SI-GaAs material.

### **III\_A.5 Role of Tunneling and Barrier Height Fluctuations**

The physics of contact injection and the possible effect of barrier height fluctuations was also probed in this study. In particular, the process of carrier tunneling as a possible mechanism for current enhancements and potential instabilities was examined. Since tunneling is a high field effect, simulations were carried out at a relatively high value of applied bias.

Simulations of the photocurrent response to a 20 ns laser pulse at different voltage ranging from 50 kV to 60 kV were carried out. The photocurrent was seen to decay for applied voltages below 55 kV similar to the behavior at the low fields. At around 58 kV, however, a persistent photoconductivity was predicted. At still higher bias, device breakdown and failure was predicted. This voltage dependent trend is consistent with the observed experimental behavior. The precise quantitative values cannot be compared, however, due to a lack of experimental data.

The above calculations took account of the Fowler-Nordheim tunneling process with a field dependent barrier lowering. However, as is well known, the effective barrier height is not expected to be spatially uniform and constant. Instead, lateral fluctuations due to the discrete nature of impurities and defects should arise. The effect of a fluctuating barrier height was incorporated by means of a simple model. The barrier height was taken to vary by 0.3 eV in a stepwise manner. Thus, half of the contact area was assigned one barrier height value, while the adjacent half was assigned another. Results of the photocurrent at a 50 kV bias exhibited a remarkable difference. The currents with barrier fluctuation were predicted to be much higher and to yield a persistent photoconductivity effect.

### III\_A.6      Role of Thermal Effects and Device Self-Heating

The results obtained here suggest the existence of a threshold for safe and stable device operation based on considerations of internal heat generation. Details of all the results obtained can be found in Ref. 13, which is included in the appendix. For single filament operation, which presents a worst scenario, no thermal instability was predicted below a power generation density level of about  $1.3 \times 10^{14}$  Watts/m<sup>3</sup>. This result is found to roughly hold under both dc and transient conditions. The prediction obtained here is in keeping with recent experimental data on PCSS devices obtained at the Sandia National Laboratory. A good quantitative match with observations was produced from the thermal simulations. Furthermore, it was shown that even for densities below the threshold, substantial device heating could result. For example, a peak internal temperature of 560 Kelvin was predicted, which represents a 87 per cent increase from the room temperature ambient value. Hence, it becomes clear that care must be exercised in incorporating temperature dependent parameters for self-consistent device simulations, even under stable operating conditions. Finally, by extending the power density threshold idea, it was argued that performance improvements and the ability to enhance the power/voltage-handling requirements for the PCSS are only possible by scaling the distance between contacts. However, at best, only a linear improvement in the performance and stability with size can result. For example, the power density is crudely given by the product of the current (I) and voltage (V), and expressed as :  $P = V I / [L A] < P_{\text{threshold}}$ , where the cross sectional area is A, while L is the longitudinal length for current flow, and  $P_{\text{threshold}}$  the power limit for stability. Since the filamentary area is roughly fixed, the only possibility for enhancing the device power handling capability is to correspondingly increase the device length L. In practice, though, since the voltage will not be evenly distributed within the device, either due to multi-dimensional geometric effects or the presence of internal traps, only a sub-linear improvement with scaling can be expected.

## IV.      Summary of work at ODU

- (1)      A two-dimensional, time-dependent numerical code was successfully, developed, tested and applied for studies of SI GaAs photoconductive switches.
- (2)      Predictions matched available low-voltage data very well. Hence, the model appears to be quite accurate in simulating the characteristics for the linear regime.
- (3)      The study suggests that use of smaller contacts placed diagonally across each other on opposite faces would enhance the hold-off voltage capability. Such an arrangement would also mitigate surface-flashover. This was probed by reducing the contact area to 30 per cent of the surface area. However, there appears to be lower limit on contact area reduction. Excessive scaling down might lead to enhanced surface fields and current crowding.
- (4)      Highly non-linear DC current-voltage characteristics have been predicted at high voltages. The shape of the curves is in keeping with that for high resistivity devices used in the past.
- (5)      No persistent conductivity or lock-on was predicted for the photocurrent response to laser pulses under low voltage dc biasing conditions. This agrees with observations of photoconductive switches operating in the linear mode. However, the internal carrier recombination time was shown to affect the magnitude and temporal shape of the current waveform. For instance, faster recombination rates resulted in current saturation, while at slower rates the photocurrent exhibited a monotonic increase during the laser excitation process.

Hence, in order to avoid lock-on or the development of potentially unstable high-current filaments : (a)

Either the optical pulses should have low intensity, (b) the optical pulse duration should not substantially exceed the carrier lifetime, or (c) a high density of internal traps and recombination centers should be present.

(6) The tunneling mechanism at the device contacts present a natural limit to the applied device voltage. Specifically, electron injection at the cathode due to this mechanism could be detrimental and lead to persistent, long-lived conductivity.

(7) Fluctuations in the barrier height can be expected to be a potential problem. It was shown that such barrier height fluctuations can substantially increase the current magnitude. Since the fluctuations depend on doping, and increase with lower doping density, the use of a thin N<sup>+</sup> layer adjacent to the cathode contact is recommended.

(8) Thermal instability was shown to be an important issue for safe and reliable device operation. A potential link between device failure and the large power dissipation within localized filaments was demonstrated.

(9) It was shown that a power dissipation density threshold for stability and safe device operation exists under both dc and transient conditions. For single filament operation, which presents a worst scenario, no thermal instability was predicted below a power generation density level of about  $1.3 \times 10^{14}$  Watts/m<sup>3</sup>. The prediction obtained is in keeping with recent experimental data on PCSS devices, and produces a quantitative match with observations.

(10) Furthermore, it was shown that even for densities below the threshold, substantial device heating can result. For example, a peak internal temperature of 560 Kelvin was predicted, which represents a 87 per cent increase from the room temperature ambient value. Hence, care must be exercised in incorporating temperature dependent parameters for self-consistent device simulations, even under stable operating conditions.

(11) Finally, by extending the power density threshold idea, it has been argued that performance improvements and the ability to enhance the power/voltage-handling requirements for the PCSS are only possible by scaling the distance between contacts. Also, at best, only a linear improvement in the performance and stability with size can result. For example, the power density is crudely given by the product of the current (I) and voltage (V), and expressed as :  $P = V I / [L A] < P_{\text{threshold}}$ , where the cross sectional area is A, while L is the longitudinal length for current flow, and  $P_{\text{threshold}}$  the power limit for stability. Since the filamentary area is roughly fixed, the only possibility for enhancing the device power handling capability is to correspondingly increase the device length L. In practice, though, since the voltage will not be evenly distributed within the device, either due to multi-dimensional geometric effects or the presence of internal traps, only a sub-linear improvement with scaling can be expected.

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13. P. Kayasit, R. P. Joshi, N. Islam, E. Schamiloglu, and J. Schoenberg, "Transient and Steady State Simulations of Internal Temperature Profiles In High-Power Semi-Insulating GaAs Photoconductive Switches," submitted for publication, J. Appl. Phys., 2000.

Research Publications Generated:

- (1) R. P. Joshi, P. Kayasit, N. Islam, E. Schamiloglu, C. B. Fleddermann and J. Schoenberg, "Numerical Studies of GaAs Bulk Photoconductive Switches for High Power Microwave Applications," J. Appl. Phys., **86**, 3833 (1999).
- (2) P. Kayasit, R. P. Joshi, N. Islam, E. Schamiloglu, and J. Schoenberg, "Transient and Steady State Simulations of Internal Temperature Profiles In High-Power Semi-Insulating GaAs Photoconductive Switches," submitted for publication, J. Appl. Phys., 2000.
- (3) R. P. Joshi, P. Kayasit, E. Schamiloglu, N. E. Islam, C. B. Fleddermann, J. S. P. Schoenberg, M. A. Richardson, and D. C. Stoudt, "Numerical Study of Optical Pulse Positioning on the High Voltage Response of SI GaAs Photoconductive Switches for High Power Applications," Proc. Pulsed Power Conference, pg. 311, June 1999.

## APPENDIX A: UNM FABRICATION REPORT

### Fabrication of PCSS at UNM for applications at Directed Energy Group, AFRL, NM

#### Objective:

UNM is expected to fabricate PCSS which is consistent with the fabrication procedures at NSWC

#### Problems:

1. Wafer Sources for UNM and NSWC
  - The parent company (Wafer Technologies, located in Europe) is the same for both the wafer sources. NSWC uses the northeast branch called the while UNM gets it wafers from Wafer Technologies at Arizona
2. Issues related to Wafer Sources
  - Both wafers have resistivity between  $1-5 \times 10^{07} \Omega\text{-cm}$  and mobility  $> 5000\text{cm}^2/\text{sec/V}$ . UNM's spec sheet (Appendix A, page 3) states 'undoped' wafer with carbon concentration between  $0.5-3.0 \times 10^{16} / \text{cm}^3$  while NSWC specification (Appendix B, page 4-6) states undoped and gives carrier concentration  $\sim 1 \times 10^{07} / \text{cm}^3$ . However since the intrinsic carrier concentration for GaAs is  $1.79 \times 10^{06} / \text{cm}^3$  it is most probable NSWC wafer also has carbon as impurity.
  - NSWC also uses wafers that are thicker than 630 um, ie 850, 1000 and 2000 um (Appendix E, Memo 1, page 12).
3. Fabrication at UNM and NSWC  
Annealing temperature, deposition of silicon nitride and contact metallization process at the two sites are different.
4. Issues with Fabrications  
There is also a difference in the annealing temperatures, which may affect device characteristics.<sup>1</sup>  
Annealing: At UNM we anneal at  $405^\circ \text{C}$ , while the devices at NSWC are annealed at  $580^\circ \text{C}$  (Reasons?: Appendix E, Memo 2,3, page 13)
5. The fabrication processes are also different at the two sites: Si<sub>3</sub>N<sub>4</sub> deposited through the PECVD process at UNM, at NSWC deposition is through sputtering. Contact metallization is through evaporation at UNM while NSWC uses RF sputtering (appendix C and D).

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<sup>1</sup> M. W. Cole et al, J. Vac. Sci. Technol. A 12(4), p1904, Jul/Aug. 1994

## **APPENDIX B - UNM Fabrication Process Description**

### **Wafer Scribing**

Three-inch GaAs wafer is scribed and cleaved into 8 PCSS devices using Karl Suss scriber.

### **Sample Clean**

1. Rinse sample in:
  - a. acetone
  - b. methanol
  - c. iso-propyl alcohol
  - d. de-ionized water
2. Blow dry with N<sub>2</sub>

### **Si<sub>3</sub>N<sub>4</sub> Layer Sides A and B**

3. Rinse in 1:30 NH<sub>4</sub>OH:H<sub>2</sub>O for 30 seconds to remove native oxide.
4. Immediately place sample in Samco PECVD chamber and pump down to approximately 10 mtorr.
5. Increase chamber temperature to 300 deg. C.
6. Initiate gas flow and deposit 1000-1500 Angstroms Si<sub>3</sub>N<sub>4</sub>.
7. Repeat steps 3 through 6 for side B.

### **Photolithography**

8. Protect backside by attaching sample to piece of Si using photoresist.
9. Repeat step 1 to clean side A/B.
10. Dehydration bake on hot plate at 120 deg. C. for 5 minutes.
11. Spin on HMDS at 4K for 30 seconds.
12. Spin on AZ5214E resist at 4K for 30 seconds.
13. Perform image reversal as follows:
  - a. Pre-bake sample on hot plate at 95 deg. C. for 90 seconds.
  - b. Transfer Rogowski contact pattern onto sample 3.5 second exposure at 365 nm.
  - c. Post-bake sample on hot plate at 112 deg. C. for 60 seconds.
  - d. Remove mask from mask holder and perform flood exposure for 60 seconds at 365 nm.
  - e. Develop in 1:4 AZ400 developer for approximately 20 seconds.
  - f. Rinse in de-ionized water.
  - g. Blow dry in N<sub>2</sub>

### **Si<sub>3</sub>N<sub>4</sub> Etch**

14. Bake sample on hot plate at 120 deg. C for approximately 5 minutes.
15. Perform O<sub>2</sub> ash removal in Tegal Plasmaline barrel etcher.
16. Perform CF<sub>4</sub> Si<sub>3</sub>N<sub>4</sub> etch in Tegal Plasmaline barrel etcher.

### **Metallization**

17. Rinse sample in 1:30 NH<sub>4</sub>OH:H<sub>2</sub>O for 30 seconds.



18. Immediately load sample into electron gun metal evaporator. Close chamber door and pump down to  $2 \times 10^{-6}$  torr. The elapsed time from 1:30  $\text{NH}_4\text{OH}:\text{H}_2\text{O}$  rinse to chamber door closure should not be greater than 10 minutes.
19. Deposit the following metals without breaking vacuum:
  - a. 200 Angstroms Pd.
  - b. 400 Angstroms Ge.
  - c. 400 Angstroms Ti.
  - d. 300 Angstroms Pt.
20. After completion of metallization, remove sample from evaporator and place in acetone for metal liftoff.
21. When unwanted metal has lifted off, remove sample and rinse in:
  - a. Methanol
  - b. Iso-propyl alcohol.
  - c. De-ionized water
22. Blow dry with  $\text{N}_2$ .
23. Repeat steps 8 through 22 for side B of sample

#### **PCSS Device Anneal**

24. Anneal sample in Rapid Thermal Annealer (RTA) at 405 deg. C. for 15 seconds in a  $\text{N}_2$  purge. Do NOT use forming gas ( $\text{H}_2$ ).

## **APPENDIX C - NSWC Fabrication Process Description**

### **Lateral, Opposed- Contact PCSS Fabrication Procedure As Performed at NSWC**

#### **.Si<sub>3</sub>N<sub>4</sub> Layer Side A**

##### **Photo-resist**

The wafer is placed onto the center of the vacuum chuck of the spinner. Then approximately 10 ml of Shipley Microposit 1813 photo-resist is dispensed onto the wafer. The wafer is then spun at 4000 rpm for 5 seconds.

##### **Soft Bake**

After the application of the photo-resist the wafer is placed on a hot plate, preheated to 115° C for 60 seconds.

##### **Align/Expose**

Now that the soft bake is completed the wafer can be patterned with the aid of a mask aligner. Align the wafer to the mask, being sure that the mask for defining the Si<sub>3</sub>N<sub>4</sub> layer is being used. Once the alignment is completed the wafer is exposed for 15 seconds to the UV light source.

##### **Develop**

Once the wafer has been exposed it is removed from the mask aligner and placed into a holder for the developer. The developer in this case consists of a beaker with enough Shipley Microposit MF-319 developer in it to cover the wafer completely when it is submerged. The beaker is then suspended in the middle of an ultra sound cleaner that is full of water. The development time is set for one minute. Once the development time has expired the wafer is removed and rinsed off with deionized water. To finish, the wafer is then dried by blowing with dry nitrogen gas making sure that both sides are dry before moving onto the next step.

##### **Reverse Sputter**

The wafer is then loaded into the RF sputtering system, which is then pumped down to desired pressure level, usually about  $5 \times 10^{-7}$  torr. Liquid nitrogen is required to get to this level of pressure. Once the desired pressure level has been achieved a reverse sputter is performed to help remove any native oxides and other minor contaminants from the surface of the wafer. This is done for 30 seconds at 100 Watts.

##### **Deposit Si<sub>3</sub>N<sub>4</sub>**

After the completion of the reverse sputter a 1000 Å layer of Si<sub>3</sub>N<sub>4</sub> is deposited onto the wafer. The RF power is set to 50 Watts and it usually takes about 25 minutes to complete the deposition.

##### **Remove Resist**

After completing of the Si<sub>3</sub>N<sub>4</sub> deposition, the wafer is removed from the RF Sputter and placed into the resist remover holding fixture. To remove the photo resist, the wafer is placed into a beaker filled with Acetone. The beaker is then suspended in the middle of an ultra sonic cleaner for 6 to 9 minutes. At the end of this procedure the wafer should have well defined exposed areas in which to deposit the contact material. After all of the photo resist has been removed the wafer is then rinsed with Acetone from a wash bottle and dried with dry N<sub>2</sub> gas. This is followed by rinsing the wafer with Methanol from a wash bottle and then dried with N<sub>2</sub> gas. The final rinse is done with deionized water and again the wafer is dried with N<sub>2</sub> gas.

#### **Si<sub>3</sub>N<sub>4</sub> Layer Side B**

Now that the Si<sub>3</sub>N<sub>4</sub> layer for side A is complete, the process for side B can begin. Use the same sequence of steps listed above to complete the B-side Si<sub>3</sub>N<sub>4</sub> layer.

## Contact Metalization Side A

### Photo-resist

The wafer is then placed onto the center of the vacuum chuck of the spinner. Then approximately 10 ml of Shipley Microposit 1813 photo-resist is dispensed onto the wafer. The wafer is then spun at 4000 rpm for 5 seconds.

### Soft Bake

After the application of the photo-resist the wafer is placed on a hot plate, preheated to 115° C for 60 seconds.

### Align/Expose

Now that the soft bake is completed the wafer can be patterned with the aid of a mask aligner. Align the wafer to the mask, being sure that the mask for defining the contacts is being used. Once the alignment is completed the wafer is exposed for 15 seconds to the UV light source.

### Develop

Once the wafer has been exposed it is removed from the mask aligner and placed into a holder for the developer. The developer in this case consists of a beaker with enough Shipley Microposit MF-319 developer in it to cover the wafer completely when it is submerged. The beaker is then suspended in the middle of an ultra sound cleaner that is full of water. The development time is set for one minute. Once the development time has expired the wafer is rinsed off with deionized water. To finish, the wafer is then dried by blowing with dry nitrogen gas making sure that both sides are dry before moving onto the next step.

### Remove Oxide

Before putting the wafer into the RF sputter the native oxide must be removed. This is done by soaking the wafer in a bath of HCl:DI Water (1:10) for 20 seconds followed by a thorough rinsing with deionized water. The wafer is then dried with dry N<sub>2</sub> gas before being placed into the sputtering system.

### Reverse Sputter

The wafer is then loaded into the RF sputtering system, which is then pumped down to desired pressure level, usually about  $5 \times 10^{-7}$  torr. Liquid nitrogen is required to get to this level of pressure. Once the desired pressure level has been achieved a reverse sputter is performed to help remove any native oxides and other minor contaminants from the surface of the wafer. This is done for 30 seconds at 100 Watts.

### Deposit Pd & Ge

After the reverse sputter a 200 Å layer of Pd is deposited onto the wafer. The RF power is set to 100 Watts and it usually takes about 25 seconds to complete the deposition. After depositing the Pd layer the wafer is positioned under the Ge target and a 400 Å layer of Ge is then sputtered onto the wafer. Again the RF power is set to 100 Watts and this usually takes 2 minutes to complete.

### Change Targets

The current NSWC sputtering system can handle only two targets at a time. Thus the Pd & Ge targets must be replaced with a Ti & Pt target respectfully. In the mean time the wafer is removed and stored in its container in a safe location so as not to be broken and/or contaminated.

### Reverse Sputter

The wafer is then loaded back into the RF sputtering system, which is then pumped down to desired pressure level, usually about  $5 \times 10^{-7}$  torr. Liquid nitrogen is required to get to this level of pressure. Once the desired pressure level has been achieved a reverse sputter is performed to help remove any native oxides and other minor contaminants from the surface of the wafer. This is done for 30 seconds at 100 Watts.

### **Deposit Ti & Pt**

Following the reverse sputter a 400 Å layer of Ti is deposited onto the wafer. The RF power is set 100 Watts and this usually takes about 3.5 minutes to complete. The wafer is then positioned under the Pt target and a 300 Å layer is deposited. This takes about 60 seconds to complete.

### **Remove Resist**

After completing of the contact deposition, the wafer is removed from the RF Sputter and placed into the resist remover holding fixture. To remove the photo resist, the wafer is placed into a beaker filled with Acetone. The beaker is then suspended in the middle of an ultra sonic cleaner for 6 to 9 minutes. This process is also known as metal lift off. After all of the photo resist and excess metal have been removed the wafer is then rinsed with Acetone from a wash bottle and dried with dry N<sub>2</sub> gas. This is followed by rinsing the wafer with Methanol from a wash bottle and then dried with N<sub>2</sub> gas. The final rinse is done with deionized water and again the wafer is dried with N<sub>2</sub> gas.

### **Contact Metalization Side B**

Since the metalization for side B is the same as that used on side A, all that needs to be done is to repeat the sequence of steps used for side A.

### **Wafer Dicing**

After all depositions have been completed the wafer is then dice up into 8 PCSS devices. The dicing operation is performed via a dicing saw. The thick samples (2 mm thick) have to be diced from both sides since the dicing blade can't cut through such a thick sample. After dicing the samples are cleaned with Methanol, dried with dry N<sub>2</sub> gas followed by a rinsing with deionized water and dried again with dry N<sub>2</sub> gas.

### **PCSS Sample Annealing**

After the samples have been cleaned they are annealed in the center of a preheated tube furnace for 5 minutes (preheated to 480° C). The atmosphere within the tube is just that, room air. The ends of the tube are sealed, but no annealing gases are used.

### **NOTES:**

1. After each development step the developer is filtered through a .2 micron filter to remove contaminants.
2. After each photo resist removal step the Acetone is filtered through a .2 micron filter to remove the particulate from the solvent. This helps keep the particulate from re-depositing back onto the wafer during later processing steps.
3. After each filtering operation the filter paper is removed and discarded. The filter holder is then cleaned and made ready for the next filtering operation.

## APPENDIX D - Correspondence

Email 1

From: bruce scott shipley <bs39@unm.edu>

To: naz@eece.unm.edu

Naz,

I got this today from Mike Richardson. If he has 0.085 cm thick devices that could explain why he gets a higher hold off voltage than I get.

Bruce

----- Forwarded message -----

From: Richardson Michael A DLVA <RichardsonMA@NSWC.NAVY.MIL>

To: "bs39@unm.edu" <bs39@unm.edu>

Subject: PCSS device thickness

Bruce,

In the paper that I wrote for the processing of the Air Force PCSS device I made reference to using 2 mm thick material. I use have three different material thicknesses that I can use, 0.85 mm, 1.0 mm, and 2.0 mm. The 2 mm thick material I can't dice from just one side because it won't cleave properly. So I dice the 2 mm thick material from both sides. The processing is the same for all material thicknesses except for the dicing operation. The .085 mm and 1.0 mm material can be diced from just one side with no problem. If you have more questions just let me know.

Michael Richardson Phone: 540-653-2716

Electronics Engineer Fax: 540-653-8029

Naval Surface Warfare Center email: RichardsonMA@nswc.navy.mil

17320 Dahlgren Road

Code B20

Dahlgren, VA 22448

Email 2

From: Richardson Michael A DLVA <RichardsonMA@NSWC.NAVY.MIL>

To: "Naz Islam" <naz@eece.unm.edu>

Naz,

480 C is the correct anneal temperature. I was annealing at 400 C early in the project, but the contacts would lift off the device. The 400 C value came from an advanced copy of a paper that the Army/Air Force were going to publish in for Pulse Power Conference 97, but the anneal temperature listed was incorrect. The final version of the paper stated an anneal temperature of 480 C. Bruce is most likely got a copy of the same paper that I had, which I think I gave him on one of my visits. I've included a corrected version of that paper as an attachment.

> -----Original Message-----

> From: Naz Islam [SMTP:naz@eece.unm.edu]

> To: A. Richardson, Michael

> Subject: Annealing

>

> Hi Mike:

> I was looking into the PCSS fab process at UNM and NSWC. Looks like you

> anneal at 480 C while Bruce does it at 405 C. Any specific reason ?

> Thanks > Naz

---

Email 3

---

Date: Thu, 7 Oct 19  
99 12:50:01 -0600 (MDT)  
From: bruce scott shipley <bs39@unm.edu>  
To: Naz Islam <naz@eece.unm.edu>  
CC: bs39@unm.edu

Naz,

The paper Mike mentions is the paper I've already seen written by Schoenburg, et al. They come up with this magical anneal temperature of 480 deg. C but they don't discuss where this temperature came from or give any references. How do I know it's not a typo.

Also, the paperwork I got from Wafer Technology LTD that came with the wafers SPECIFICALLY states "Decomposes to evolve arsenic vapour if heated above 480 degrees C."

I'm sticking with 405 deg. C  
Bruce

## **APPENDIX E: IEEE Transactions on Plasma Science (Under review)**

### **COMPENSATION MECHANISMS AND THE RESPONSE OF HIGH RESISTIVITY GaAs PHOTOCONDUCTIVE SWITCHES DURING HIGH POWER APPLICATIONS<sup>2</sup>**

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**Abstract--** Photoconductive semiconductor switches (PCSS) made from semi-insulating (SI) GaAs are the prime switching component of one class of high power, ultra-wideband (UWB) microwave sources. The high resistivity of the GaAs can be obtained through different processing techniques. The resultant device characteristics of the PCSS such as breakdown voltage, rise time, and turn-on delay will depend on the actual processing technique that was used for the GaAs. Simulation studies comparing an intrinsic material and a high resistivity SI GaAs PCSS grown through the liquid encapsulated Czochralski (LEC) process with a deep donor and shallow acceptor compensation mechanism highlight these differences. Simulations also elucidate the role of an  $n^+$ -doped layer placed next to the cathode, which increases the breakdown voltage of the device; extending the  $n^+$  layer length beyond the cathode does not yield further improvement, but leads to current confinement along a narrow strip that can initiate local heating or burnout. The doping profile of the  $n^+$  layer also affects hold-off characteristics, a faster gradient ensuring better protection of the cathode against the substrate field and electron injection. Doping the  $n^+$  region with a higher concentration of carbon impurities does not produce the same effect as the  $n^+$ -SI interface. These material-related issues are critical to extending the performance characteristics of PCSS's.

**Index Terms--** PCSS, ultra-wideband microwaves, fast semiconductor switching.

#### **Introduction: High Power Switching**

Even though they are a high resistivity semiconductor material with very little free carriers for conduction, semi-insulating (SI) semiconductors have been used in applications other than as an isolation region between active devices. Applications include charged particle detectors, drivers for lasers, and as high impedance low current Q-switch or Pockel cell [1-2]. Another important use of this material is as a closing photoconductive semiconductor switch (PCSS) in a setup for generating ultra wideband (UWB) high power microwave (HPM). Some of the advantages these switches offer compared to conventional switch include improved jitter, better inductance matching, compact size, and in some cases, lower laser energy requirement for switching action. A specially designed and modified version of the PCSS, using refractory metals and a Rogowski-profiled contact on the front and back (opposed contact) of the wafer, has been successfully used in generating UWB HPM radiation with improved risetime and hold-off characteristics [3]. Gallium Arsenide

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(GaAs), because of its properties that are conducive to faster switching action, has been primarily used as a material of choice in this application where fast, repetitive switching action is required [4].

High resistivity GaAs semiconductor material may be of the intrinsic (pure) form or of the compensated type. In both cases the resistivity can exceed  $1 \times 10^{07} \Omega\text{-cm}$ . However, even though the free carrier concentration and resistivity values may be the same, the PCSS's response will be different for the intrinsic semiconductor and for the variety of compensated materials fabricated through techniques involving a compensation mechanism between predominant defect states [5-8]. The three most widely used compensation processes, as shown in Figure 1, are the (A) deep donor shallow acceptor (DDSA) compensation process, (B) shallow donor deep acceptor (SDDA), and (C) deep donor deep acceptor (DDDA). The DDSA type material is grown through the liquid-encapsulated Czochralski (LEC) method where a balance is achieved between the deep lying EL2 donor defect and a residual shallow acceptor impurity, usually carbon (C). The SDDA material is produced by what is known as the Horizontal Bridgman (HB) technique, where SI compensation is obtained by doping the melt with chromium (Cr), resulting in deep level acceptors. This deep level acceptor compensates any residual shallow donor (e.g., Si). Finally, when the Si content is reduced below the normal EL2 level, a compensation mechanism between the deep EL2 donor and deep Cr acceptor brings about the DDDA material. In this article we present simulation results and analysis of an opposed-contact PCSS shown in Figure 2 (top). The switch material is the DDSA-type and has been used for sometime for generating ultra-wideband high power microwaves. Specifically, conditions at high bias is compared with a high resistivity intrinsic material PCSS of similar configuration. Methods for improving the breakdown characteristics are also discussed and the rise time for the two switch types are compared.

### Simulation tool And Mesh Setup

Simulations were performed out using the SILVACO software for semiconductor studies [9]. This is a comprehensive tool that can perform semiconductor device process and circuit simulations, and includes numerous models and parameters that can be defined for any specific situation to obtain the best results possible. The code, with a main interface (ATLAS) and other interactive tools, provides for a 2- and 3-D semiconductor device simulation that also includes thin film transistors (TFT), quantum devices, heterostructures, and power devices. The device to be simulated can be "fabricated" using the ATHENA process module interfaced with ATLAS, and the resulting mesh can be used for simulation. Furthermore in a "mixed-mode" environment the device can be placed in a circuit and the effects of any changes in the device parameters on the overall circuit can be studied. In addition to the drift-diffusion model, one can study such "non-local" effects as velocity overshoot, reduced energy-dependent impact ionization, *etc.* using the energy balance model wherein such transport parameters as mobility and impact ionization become functions of the local carrier temperature rather than the local electric field. Finally, the code also has a provision to incorporate user-defined functions through a C-interpreter. The simulation provides a self-consistent solution of Poisson's equation and the continuity equation, describing the variation in electrostatic potential with local charge densities. The evolution of electron and hole densities due to transport, generation, recombination, *etc.* can be later plotted for analysis. Details about the code and the equations are provided in [10].

The GaAs PCSS used in the simulation was generated through an interface with the BLAZE module which simulates III-V semiconductor devices. A SI-GaAs PCSS simulation mesh, with contacts on the front and back of the wafer (opposed contacts), very similar to the one used in Ref. 2, was generated for this study. As shown in Figure 2, the shortest distance between the contacts is about 0.25 cm and the contact material is Pd, whereas in the actual device, layered Pd/Ge/Ti/Pt of thickness 200/400/400/300 Å, respectively, were used. The device dimensions are 2700 x 630  $\mu\text{m}$  whereas the actual device is 2 cm x 1.3 cm x 630  $\mu\text{m}$ , detailed in [10, 11]. Since the simulation mesh has the same distance (0.25-cm) between the contacts as the actual device, it is expected that the truncation of device dimensions, especially the contact length, will not affect the physics associated with the device. Also, Pd as the contact material is expected to provide the basic physics associated with the contact (work function, *etc.*). Simulations include i) the effects of the length of the  $n^+$  region, on the transport characteristics, ii) doping profile of the  $n^+$  region, and iii) effects of SI-material type on device rise time and rise time delays.

### Simulation and Results



For a LEC grown DDSA switch (Figure 2), initial improvements in the hold-off characteristics were achieved through changes in the contact itself, as reported in [3]. This included changes in i) the contact position (opposed contact), ii) its profile (Rogowski) and, iii) material (refractory metals). Further improvements in the rise time for the device could be possible when it is operated at a higher field. Further increase in terminal voltages, without increasing the distances between the contacts, however, results in premature breakdown of the switches [11-13]. Eliminating this cause for early breakdown may result in higher bias operation that may lead to faster rise time, and hence increased energy transfer to the load during switching.

One reason for premature breakdown may be attributed to changes in the material characteristics during device operation. This is true for the DDSA type material where the filling of EL2 traps (Figure 3) and the subsequent inhomogeneous nature of the device affect switching beyond a certain voltage [10]. Trap-filled regions are formed near the cathode initially, spreading to the anode later, and ultimately interfering with the conduction mechanism. Thus, one way of improving the device hold-off characteristic is to shift the formation of the trap-filled regions to higher voltages. This is possible through mechanisms that would suppress electron injection until higher bias ( $> 34$  kV) is reached. Simulations of the structure with an  $n^+$  region next to the cathode shows marked improvements in the operating voltage of an opposed-contact DDSA-type switch. The reason for such a response may be attributed to the interaction between a SI layer and an  $n^+$  region adjacent to it. As detailed in [10, 13] the introduction of a  $20 \times 200 \mu\text{m}$ ,  $10^{18} / \text{cm}^3$  doped  $n^+$  region has two important effects: i) it shifts the high field region from the contact to a region near the  $n^+$ -diffused layer and, ii) it lowers the high field near the contact. The nature of a  $n^+$ -SI contact also results in inhibiting electron injection until higher bias is reached [10]. As a result, there is no trap-filled region next to the cathode (Figure 4), and device breakdown does not occur until much higher bias. This is in contrast to Figure 3, which shows a large trap-filled region next to the electrodes and is for the structure without an  $n^+$  region next to the cathode. In order to characterize the  $n^+$  region in terms of optimum thickness, length, and nature of doping profile, and to determine critical parameters that affect the hold-off characteristics of the opposed-contact, PCSS simulations were carried out with various lengths and depths of the  $n^+$  region.

Figure 5 shows the simulation results for the switch with the  $n^+$  region spread along the surface on the cathode side. The current-voltage (I-V) trace shows better hold-off characteristics than a device without the layer, and is similar to that of a  $200 \times 20 \mu\text{m}$  of  $n^+$  layer beyond the cathode contact. Although this configuration is easier to process (it is easier to deposit a layer all a surface than along a measured length of the device), the current distribution in the bulk, however, is not homogenous. Rather, a large current density is confined to a column perpendicular to the anode. This not only increases the possibility of local temperature effects, but increased trap-filled regions at one location may make the device characteristics inhomogeneous, which is detrimental to device operation and its lifetime. Simulations with the  $n^+$  region occupying half the device length shows some improvement (not shown here), but a short  $n^+$  length perhaps provides the maximum benefit.

Effects of compensation mechanism on the hold-off voltages were also studied by changing the compensation of the SI region. Figures 6 show the case where the acceptor (Carbon) concentration is increased to  $5 \times 10^{15} / \text{cm}^3$ , much above the EL2 level of  $3 \times 10^{15} / \text{cm}^3$ . The device is effectively low-doped p-type. The breakdown voltage is not increased as a result. The region in this case is basically a forward-biased p-n junction that facilitates minority carrier injection whereas in the case of the  $n^+$ -SI region, the resulting field inhibits electron injection and the EL2 levels act as traps for injected electrons. Hence, there was no change in the I-V characteristics when the doping of the  $n^+$  region was increased by an order of magnitude.

Figure 7 shows a large area of recombination sites for the intrinsic PCSS soon after the application of voltage. As discussed in the next section, intrinsic semiconductors are also known as relaxation materials (relaxation time/Debye length is comparable to the carrier lifetime/Diffusion length), where initial inje

ction of minority carriers is accompanied by recombination with the majority carriers. This is in contrast to doped lifetime materials (relaxation time/Debye length is small compared to the carrier lifetime/Diffusion length) where majority carriers (to maintain charge neutrality) augment the injected minority carriers. Following initial recombination, the drift-diffusion process sets in and the I-V characteristics is similar to the compensated PCSS. As the bias is increased and the minority carriers are near the background level, recombination near the cathode (Figure 8) brings about a decrease in the current. The I-V plot in Figure 9 shows this at a bias of 8 kV. This is also evident in the rise time profile of the PCSS pulses following the switching action, as shown in Figure 10, which shows kinks for the intrinsic PCSS. When the rise time is in the sub-nanosecond timeframe, intrinsic or very low-doped PCSS may thus introduce delays in the switching process as compared to compensated material.

## Discussion And Summary

High resistivity SI GaAs PCSSs are either intrinsic or made through a compensation process. Carrier transport in intrinsic or relaxation materials (as in most low doped semiconductors) is different from transport in doped lifetime semiconductors [15,16]. Compensated SI GaAs materials, on the other hand, have some characteristics of doped semiconductors. Thus, the rise time, I-V characteristic and other parameters are different in high resistivity materials made through different processes. It depends to a large extent on whether the material is intrinsic or compensated. Rise time effects are critical for devices requiring sub nanosecond pulses.

For undoped SI materials that are fabricated through compensation mechanism, the presence of a high concentration of traps results in a substantial depletion of injected carriers, and trap-filled regions begin to affect the device's response, especially at high biases. The properties of compensated SI GaAs and the process involved in fabricating it play an important role in determining the breakdown and other device characteristics. The device response will be different for the deep donor shallow acceptor type of material (EL2-Carbon compensated, DDSA-type) when compared to the intrinsic or the shallow donor deep acceptor type material (Silicon and Chromium compensated).

Deposition of an  $n^+$ -doped region next to and covering the cathode (in a DDSA type material) improves its breakdown characteristics. Electron injection and the formation of trap-filled regions then occur at a higher bias, thereby increasing the breakdown voltage of the devices. Increasing the length of the doped region does not contribute to improving the hold-off characteristics, but is detrimental to the current density and may lead to local heating and the device's ultimate failure. Increased doping of the  $n^+$  region does improve the device response somewhat, but the effect saturates as degeneracy is reached. Increasing the carbon concentration does not improve the hold-off characteristics. For high power PCSS analysis it is therefore important to understand the underlying fabrication processes in order to correlate it with the devices' behavior.

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FIGURES for APPENDIX E

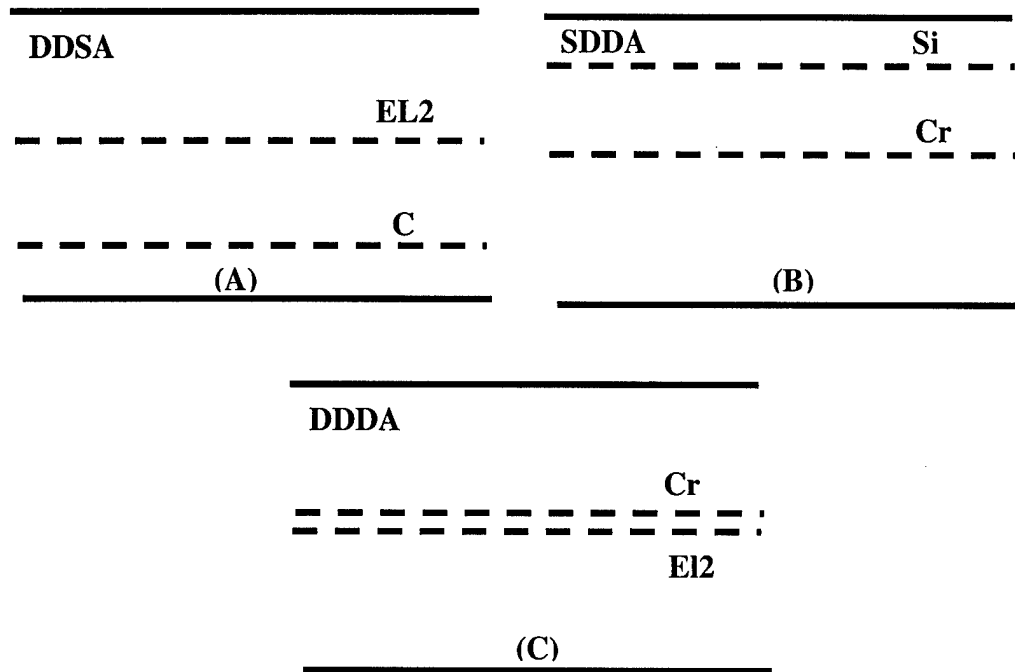


Figure 1: Energy level diagram for the three compensation mechanisms for semi-insulating GaAs PCSS

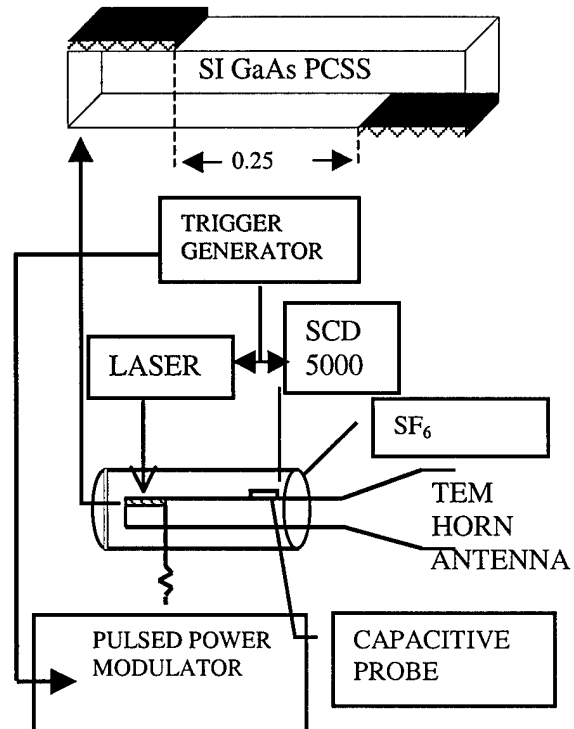


Figure 2: Experimental setup for generating Ultra Wide Band radiations using GaAs PCSS (also shown on top).

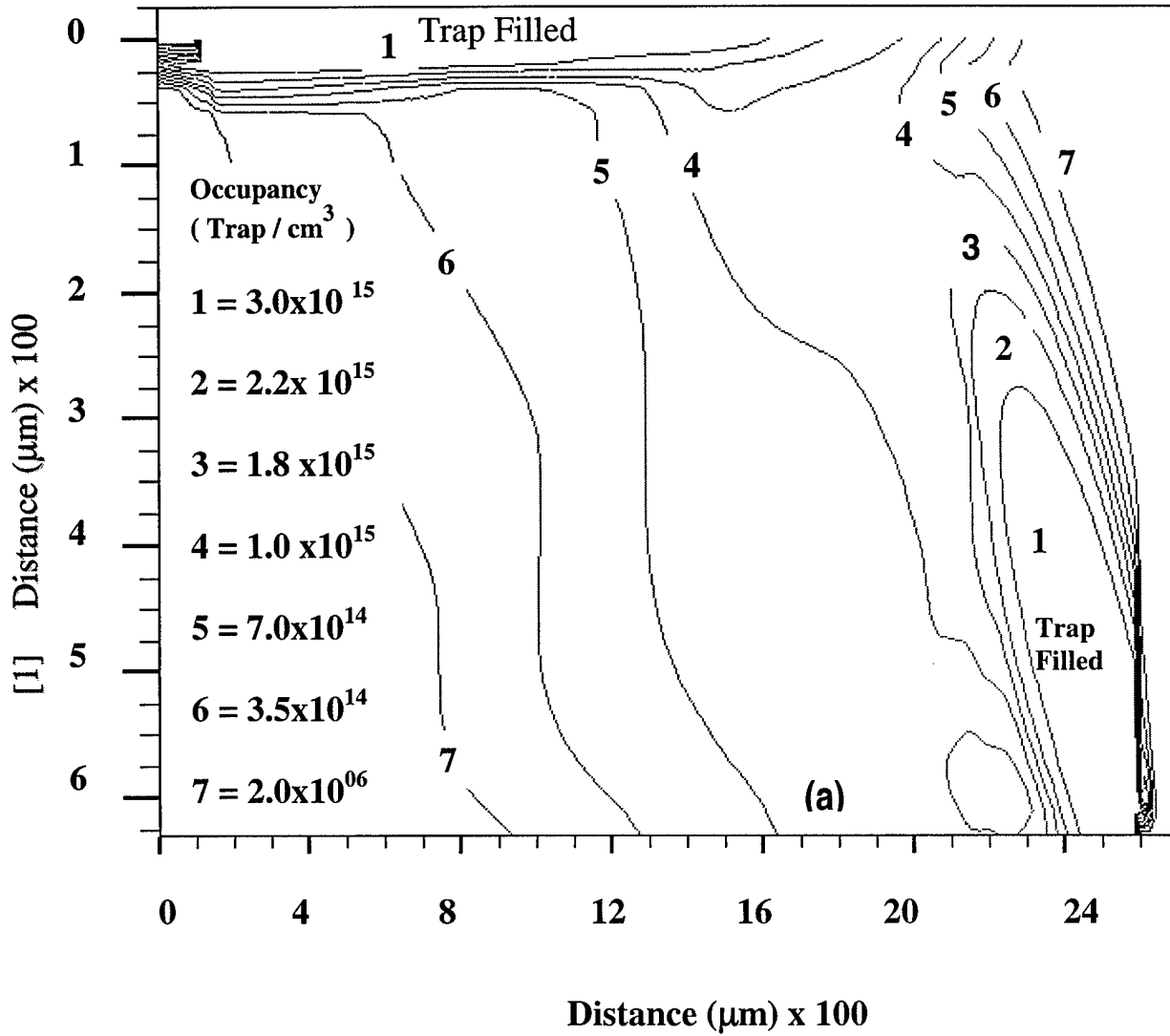


Figure 3: Trap filled regions near the electrodes at high bias prior to breakdown.

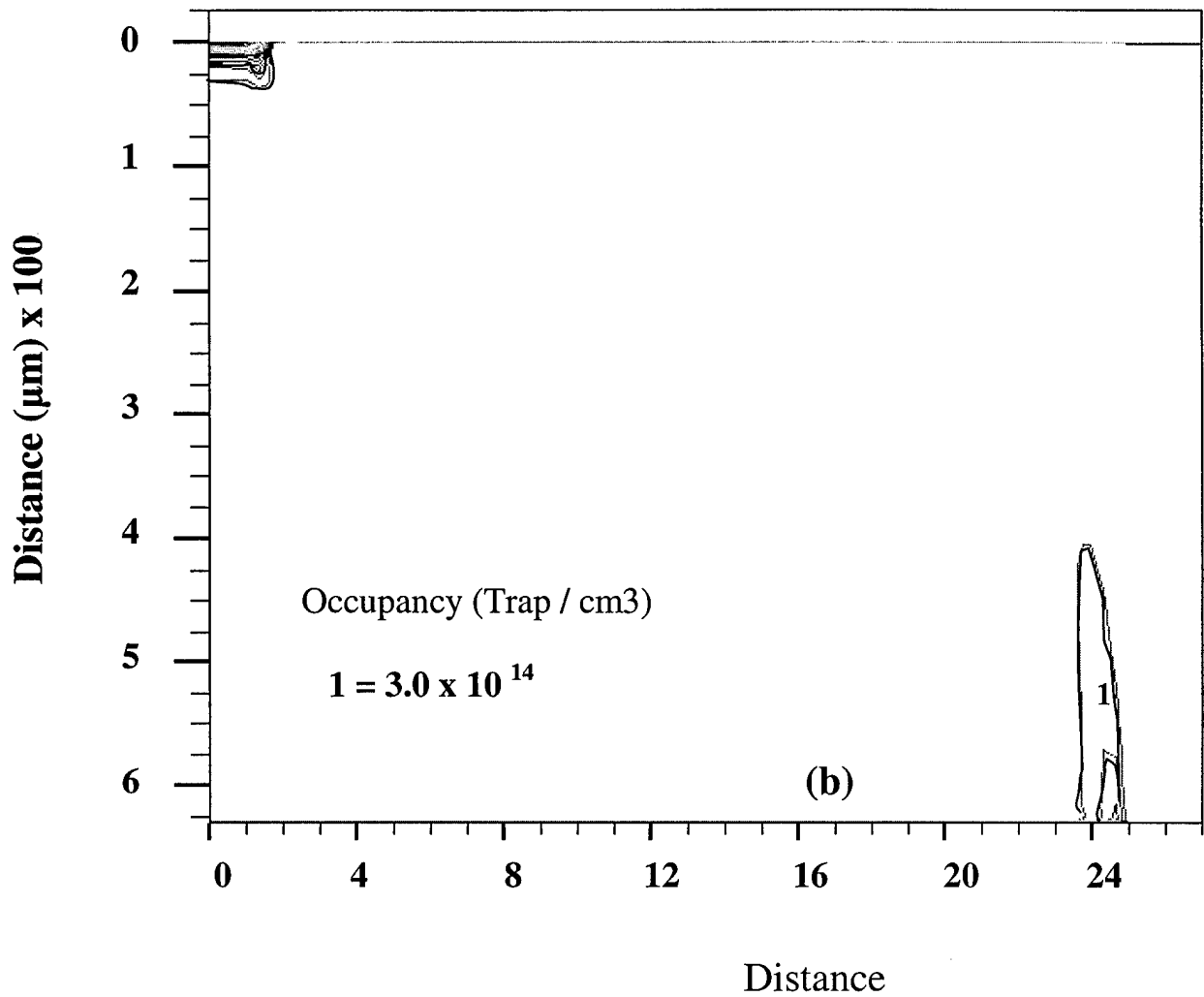


Figure 4: Trap concentration at high bias with an  $n^+$  region next to the cathode. These regions inhibit electron injection from the cathode.

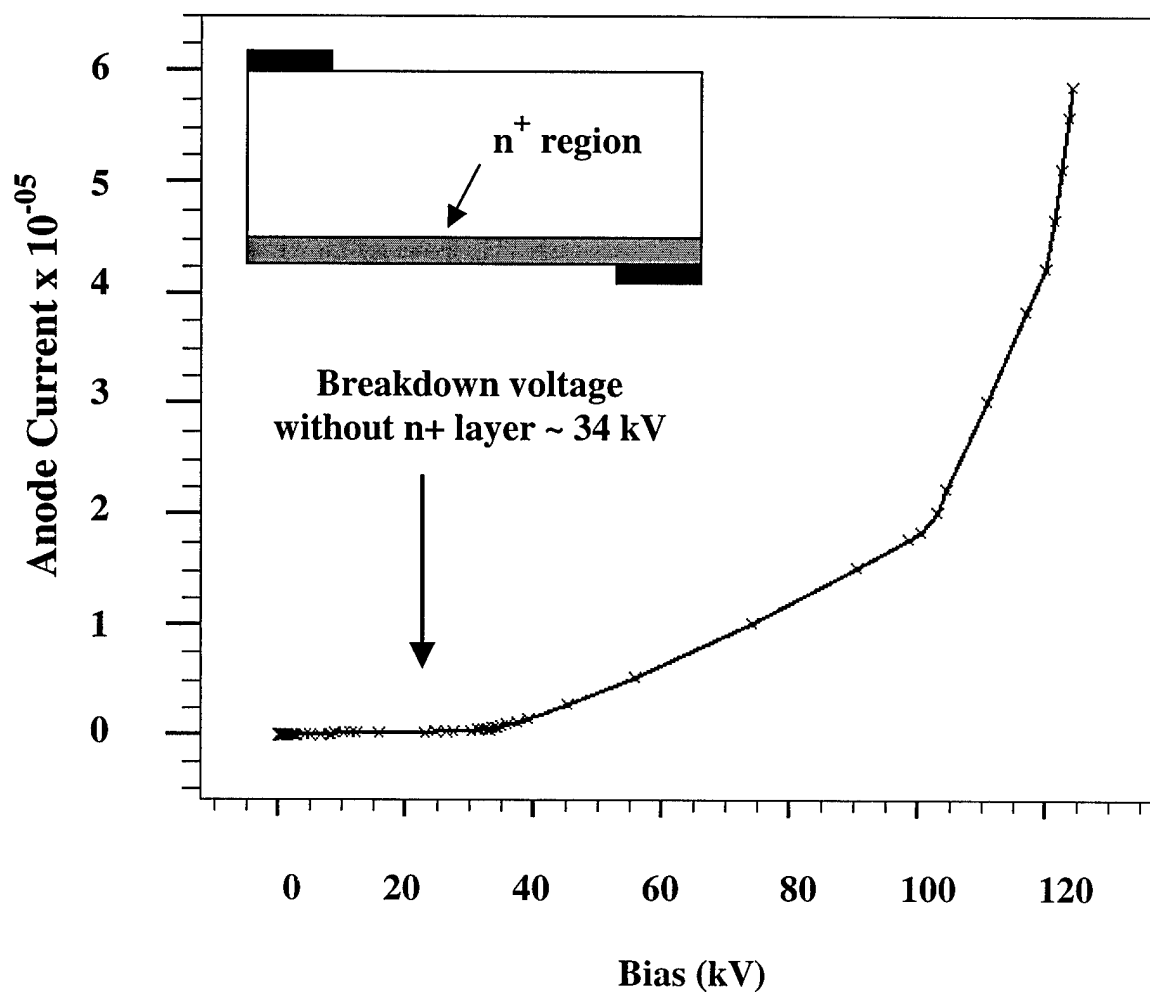


Figure 5: I-V characteristics with the n<sup>+</sup> region along the cathode side. This configuration limits current flow to a small region, which may affect local heating.



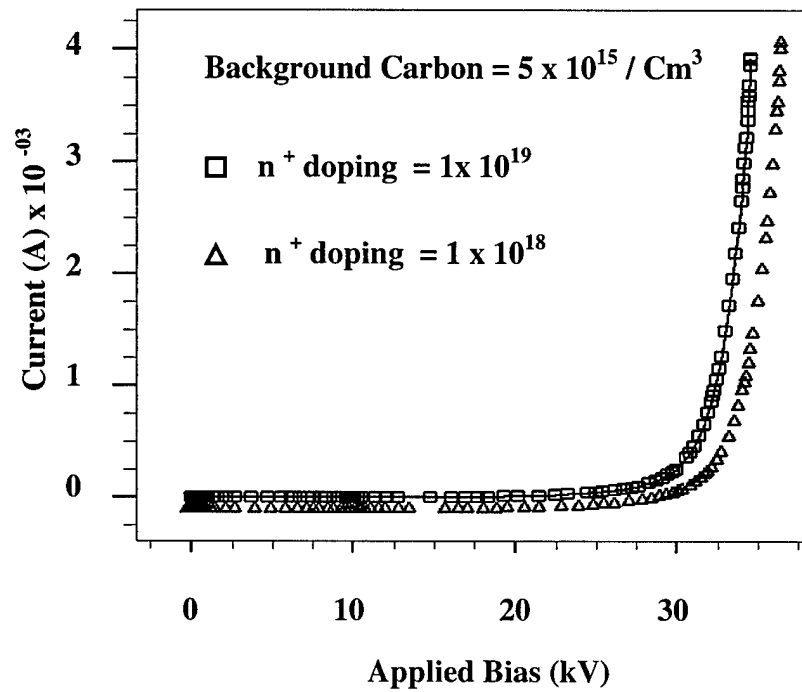


Figure 6: I-V characteristics with increased background doping. The breakdown voltage does not increase with  $n^+$  doping when the effects of traps are minimized.

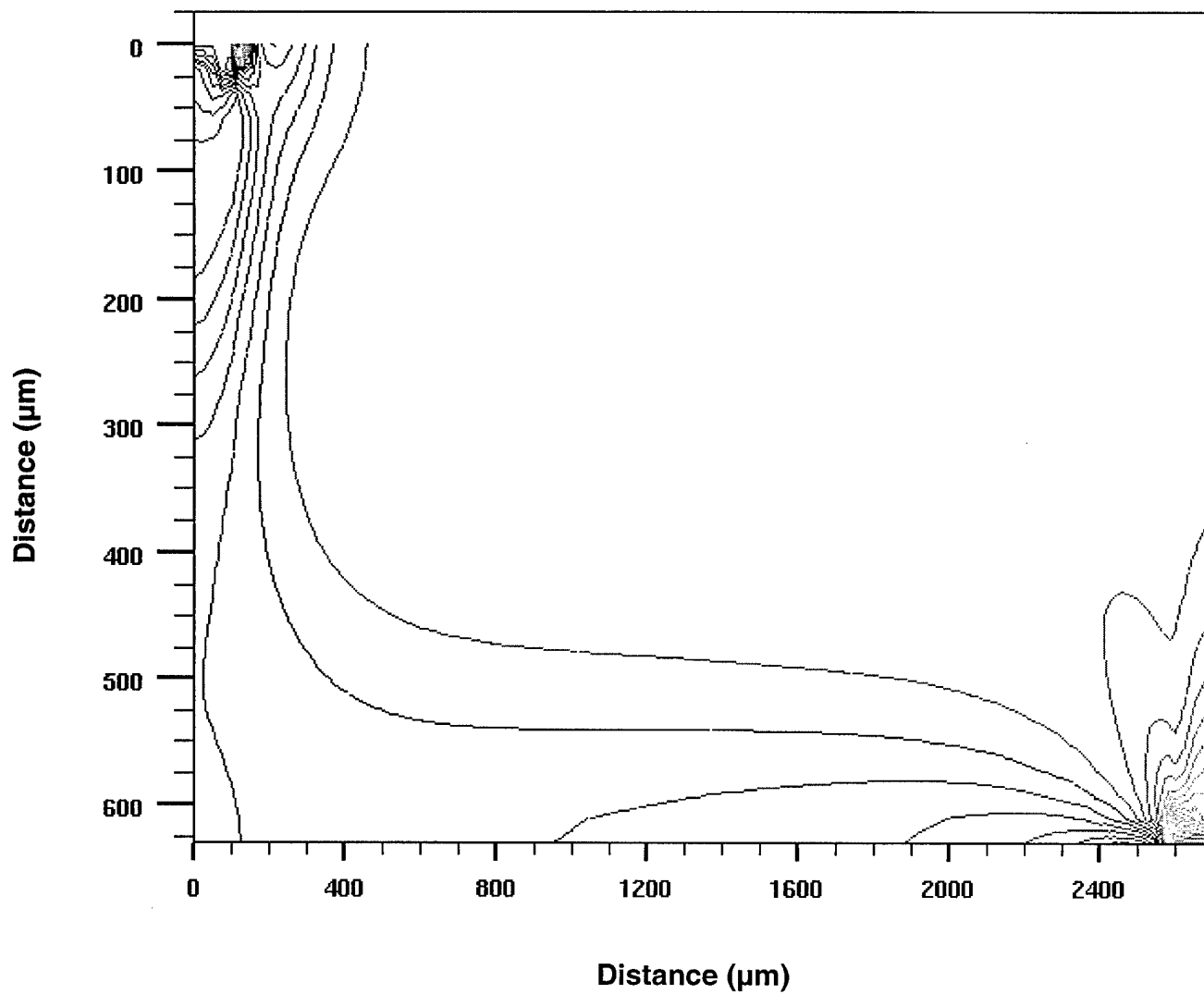


Figure 7: Initial recombination sites at low bias. This may effect the initial rise time for intrinsic material.

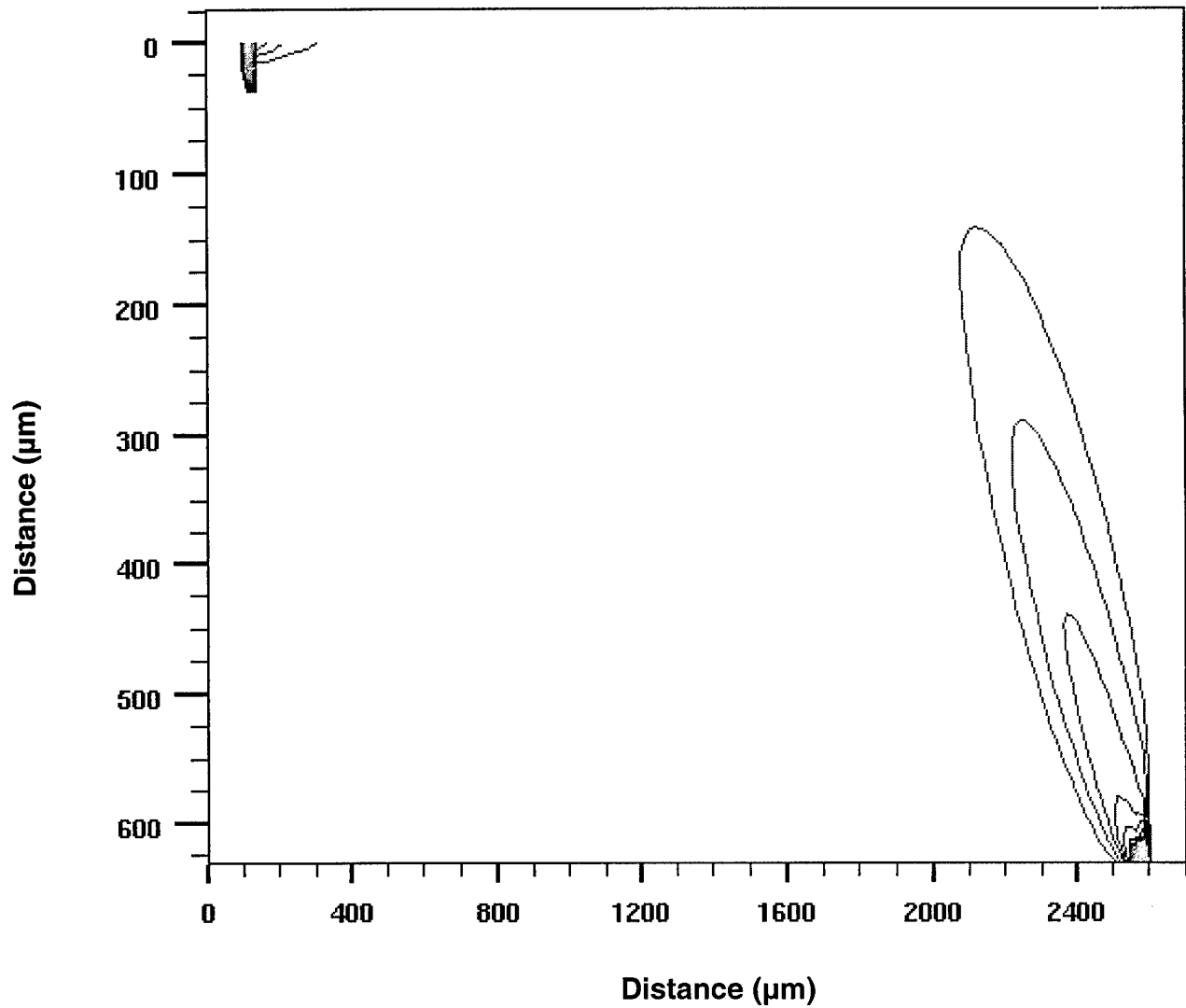


Figure 8: Recombination near the cathode at high voltage, which results in the reduction of current.

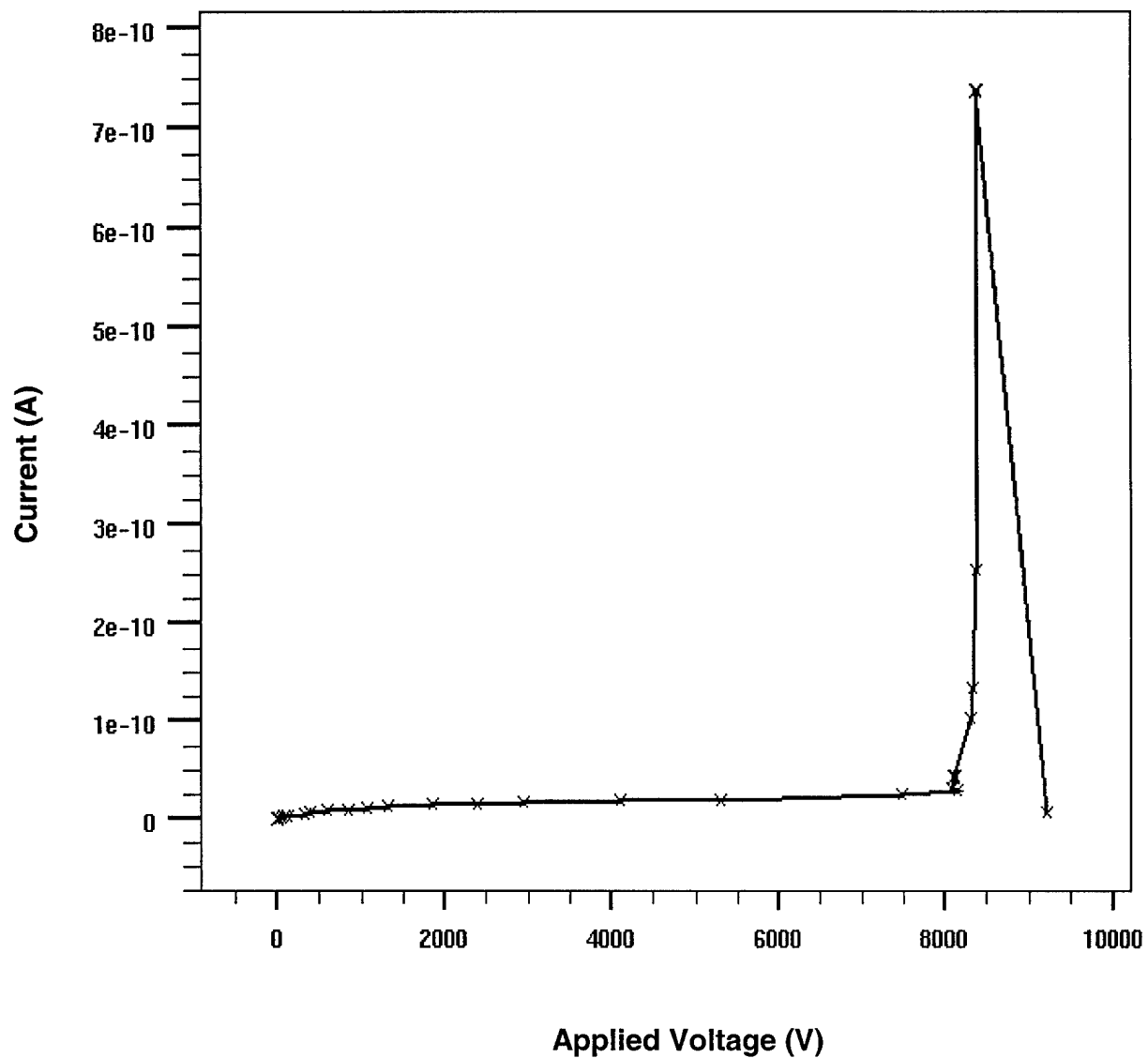


Figure 9: I-V characteristics for the intrinsic material. A change in the recombination results in initial decrease in current and spikes as seen in figure 10.

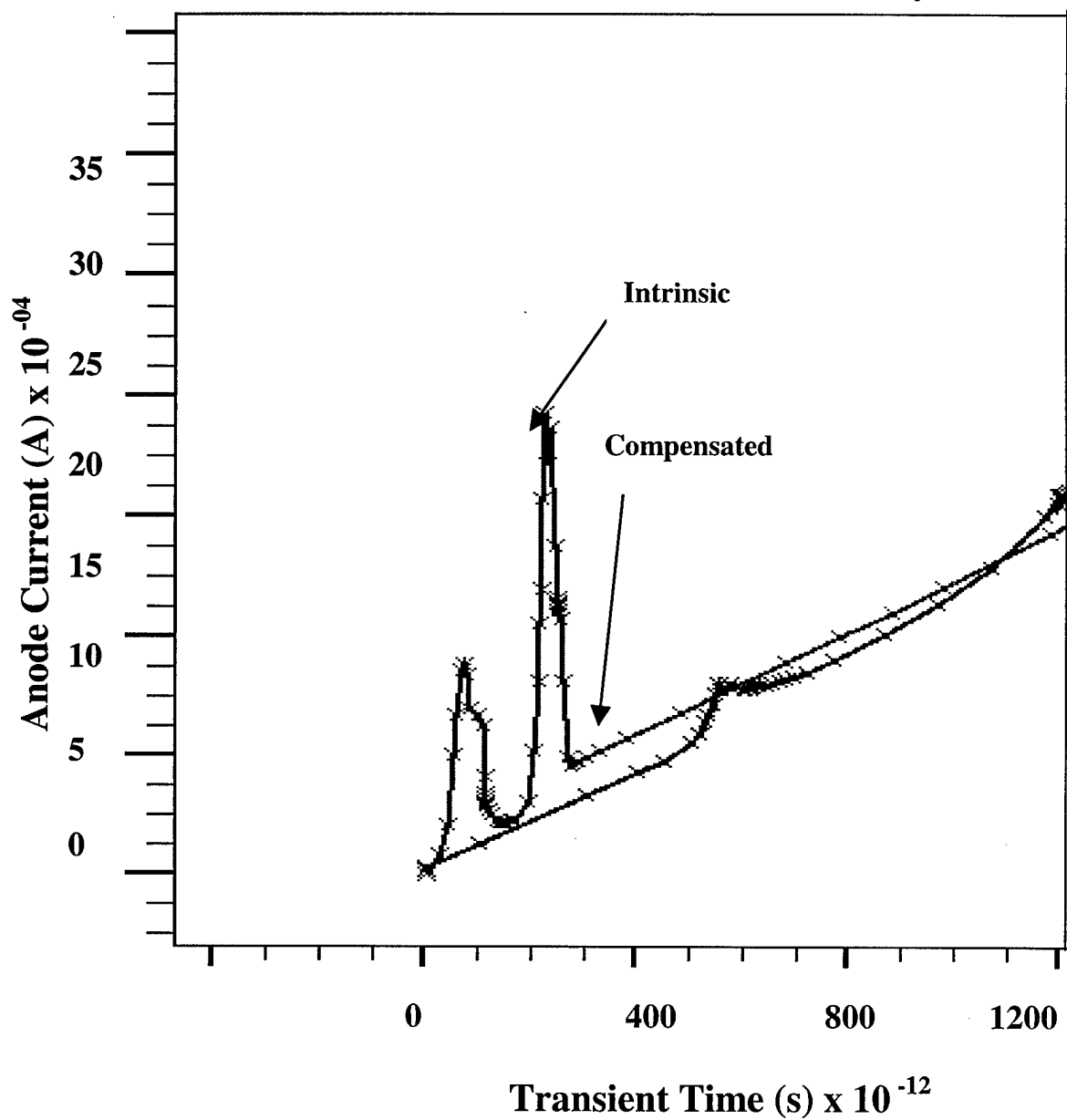


Figure 10: Spikes in the intrinsic material may effect rise time of the PCSS specifically in the sub-nanosecond regimes.

**APPENDIX F: Paper submitted to the Journal of Applied Physics**

**TRANSIENT AND STEADY STATE SIMULATIONS OF INTERNAL TEMPERATURE  
PROFILES IN HIGH POWER SEMI-INSULATING GaAs PHOTOCONDUCTIVE SWITCHES**

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**ABSTRACT**

Simulations have then been performed to determine the internal temperature profiles of high-power GaAs photoconductive switches in the presence of a current filament. No thermal instability is predicted below a power generation density level of about  $1.3 \times 10^{14}$  Watts/m<sup>3</sup>. This prediction is in keeping with recent experimental data on PCSS devices. It is shown that this power dissipation density threshold for stability exists under both dc and transient conditions. Based on the power density threshold idea, it is argued that enhancements in the power handling capacity can only scale sub-linearly with increasing contact separation.

## INTRODUCTION

High resistivity semiconductors are used in a variety of applications that include charged particle detectors, drivers for lasers, as regions of electrical isolation between active semiconductor devices, and in high impedance low current Q-switches or Pockel cells [1-2]. In addition, such material is also used to fabricate closing photoconductive semiconductor switches (PCSS). The PCSS offers several inherent advantages over conventional switches that include the provision of a jitter-free response, better inductance matching, compact size, fast rise times, and in some cases, lower laser energy requirement for the switching action. The PCSS functions as a basic switching element that is rugged and tolerant to large voltages and high power input signals. It is typically embedded within the overall electrical circuits, and find utility in applications ranging from the generation of ultra wideband (UWB) high-power microwaves (HPM), frozen waveform generators, direct current to radio frequency conversion circuits, high-frequency plasmatrons, and impulse radar systems [3, 4]. In particular, semi-insulating (SI) GaAs material has been developed in the recent past for PCSS-based pulsed power technology and high voltage applications [5-12]. The high resistivity GaAs semiconductor material may be of the intrinsic (pure) form or of the compensated type [13-18]. In both cases, the resistivity can exceed  $10^7 \Omega\text{-cm}$ . Advantages of the optically-triggered GaAs switches include: fast rise-times in the 200 ps range, an extremely high power delivery capacity with currents in the kilo-Ampere range and voltages beyond 100 kV, kilohertz and megahertz operation in the continuous and burst modes, respectively, optical control with adequate isolation, and device scalability. For example, a specially designed and modified version of the PCSS, using refractory metals and a Rogowski-profiled contact on the front and back (opposed contact) of the wafer, has been successfully used in generating UWB HPM radiation with an improved rise-time and hold-off characteristics [19]. Of practical importance, is the ability of these switches to operate in a "non-linear" mode at high values of the applied bias. This high-gain non-linear mode was first observed by Williamson et al. [20], and turns out to be highly energy efficient.

Despite the promising trends, this technology has not quite matured, and a number of unresolved problems remain. For example, in experiments, PCSS devices have exhibited high pre-breakdown currents, displayed softer breakdown thresholds, and often displayed unstable electrical behavior. At high device

voltages, the conduction capacity does not appear to be limited by the photon flux, and a persistent photo-conductivity effect is observed. This is indicative of an internal voltage-dependent charge generation mechanism. The formation of current filaments within the PCSS leading to overall device failure has also been reported. Since this is highly detrimental to device reliability and overall system stability, it is necessary to understand the underlying physics for control and suppression of the internal instabilities. Different mechanisms have been invoked for explaining some of the observed features [21-25]. For instance, avalanche ionization [26], field-dependent trap filling [27], double injection [25], recombination radiation [22], and streamer formation [21] have been some of the processes considered. The role of recombination radiation, its transport and subsequent non-uniform absorption was studied by Stoudt and Kushner [22]. In previous studies by our group, the role of internal inhomogeneities [28], doping variations and effects arising from deep defect levels associated with the compensation mechanisms [29, 30] have all been analyzed. An important point to recognize in this regard, though, is that all of the above studies and analyses have *neglected device self-heating*. It has implicitly been assumed that the electrical properties of the PCSS under high-voltage, high-power operation remain unchanged, and the transport parameters can adequately be represented by their ambient values.

Here, we examine thermal effects in PCSS devices. The thermal issue is especially important in the context of PCSS, since primarily, these devices are candidates for high-power, high-voltage applications. Large internal Joule dissipation and self-heating is expected to be the norm under continuous device operation conditions. Unfortunately, the device temperature and the ability to disperse the internal heat are controlled by the thermal conductivity parameter,  $\kappa$  which is temperature dependent. The conductivity  $\kappa$  depends on an effective phonon relaxation time  $\Phi_{pr}$  which is shaped by the combined effects of the various phonon processes [31,32]. These typically include normal three-phonon processes [33,34], boundary scattering [35,36], isotope/point defect interactions [37], and the Umklapp mechanism [38, 39]. If the operating temperatures are not very low the value of  $\kappa$  begins to *decrease* monotonically with temperature due to increases in the combined phonon scattering rate (i.e. less efficient heat transport and removal.) For bulk GaAs, this regime of decreasing thermal conductivity would be encountered for operation at temperatures of 300 K and beyond. Experimental studies on GaAs confirm this monotonically decreasing



trend in thermal conductivity [40-42], and reveal an approximate  $T^{-n}$  functional form, with  $1 < n < 2$ . Though the precise cause for PCSS failure remains somewhat unclear, secondary breakdown arising from thermal causes remains a likely and unexplored process.

Current filamentation within a PCSS, as has been observed in experiments [5, 7], presents another scenario in which thermal effects would assume great significance. In the event of filamentation, the power dissipation density is expected to become very large and strongly non-uniform. This could then lead to severe increases in local temperature, augmented by the feedback effect associated with the negative differential thermal conductivity. The technological implications are obvious. The occurrence of highly localized power dissipation as in current filaments, coupled with the strong conductivity decreases with temperature, could lead to catastrophic and irreversible failures in PCSS devices. This possibility has not been quantitatively analysed to the best of our knowledge. It is important to evaluate the conditions favoring such breakdown and the operating parameter space that could trigger device failures. The region for safe device operation from a thermal standpoint is not well known, and suitable bounds for PCSS reliability have not been established. Here, we begin an attempt to address this complex issue.

Changes in the internal device temperature are also expected to affect the stability of operation. For example, with an increase in temperature, the phonon assisted detrapping rate will increase. This implies that local hot-spots can thus serve as mechanisms for triggering inhomogeneous internal current densities by releasing trapped charge. It may also be pointed out that a monotonic increase in the ionization coefficients with temperature has also recently been observed in SiC material containing dislocations and defects [43]. Since Si-GaAs is known to contain impurity states and defects, a similar enhancement in impact ionization with temperature leading to instability is likely and logical. Given the sensitivity of the various parameters on the internal temperature and the potential effects on device stability, thermal simulations have been performed in this contribution for PCSS devices. The primary goal is to ascertain the peak temperature and internal profiles under both transient and steady state conditions in the presence of a filamentary current. The filamentary scenario presents an important case study, since the PCSS under high-voltage, low optical excitation conditions typically operates in this mode for maximum efficiency. Besides, it represents the worst scenario for stability analysis. In this contribution, we also attempt to determine a heat generation density threshold for stable device operation under filamentary conditions. Finally, variations in internal temperature

under cw device operation have also been analyzed. Numerical solutions to the three-dimensional thermal diffusion equation were obtained by utilizing the heat diffusion equation and the Kirchoff transform to determine the internal temperature profiles. Experimental temperature-dependent thermal conductivity measurements available from the literature were used in the calculations.

### SIMULATION DETAILS

A sketch of the equivalent device structure used for the simulations is shown in Fig. 1. The size and dimensions were chosen to roughly equal those of actual device structures that have grown and tested [25,30]. The actual switch dimensions were 1.0 mm along the radial direction, and 2.5 mm along the longitudinal axis as shown in Fig. 1. The choice of a cylindrical geometry for simulation work was guided by a desire to maintain structural simplicity since current filaments that produce internal heating are known to have a cylindrical shape. Simple contacts were assumed on the two opposite faces in the x-y plane with current flow (and hence filament formation) along the perpendicular z-direction.

The internal device temperature was obtained by solving the diffusive heat flow equation for assumed heat generation profiles. This heat flow equation contains a source term to account for the internal power dissipation within the simulation volume. In the present case, this would physically arise from filamentary current flows. In cylindrical coordinates, the requisite equation for the thermal problem is given as :

$$\nabla \cdot \{kT \nabla T\} + g = \Delta C_p MT/Mt \quad , \quad (1)$$

where T is the temperature, g the heat generation function, k the temperature dependent thermal conductivity,  $\rho$  the GaAs density, and  $C_p$  the heat capacity. In cylindrical coordinates, equation (1) becomes:

$$\begin{aligned} & (1/r) M[kr(MT\{r,2,z,t\}/Mr)]/Mr + (1/r^2) M[k(MT\{r,2,z,t\}/M2)]/M2 + \\ & + M[k(MT\{r,2,z,t\}/Mz)]/Mz + g\{r,2,z,t\} = \Delta C_p MT\{r,2,z,t\}/Mt \quad , \quad (2) \end{aligned}$$

Due to the temperature dependent conductivity, the above equation is non-linear, and so does not lend itself to analytical solutions. Often the non-linearity is ignored by assuming  $dk[T]/dT = 0$ . Here, we retain a temperature dependent thermal conductivity. The temperature dependent thermal conductivity  $k(T)$  was taken from a recently published experimental report for SI-GaAs with values in the 300-800 K range [40-42].

The parameter  $k(T)$  can be approximated by the following curve:  $k(T) = 76 - 0.1 T \text{ Wm}^{-1}\text{K}^{-1}$ . Thus, at room temperature a  $46 \text{ Wm}^{-1}\text{K}^{-1}$  value is predicted by the above expression. The governing differential equation (2) was solved using a finite difference method. The uniform grid chosen had mesh sizes of  $\Delta z = 12.5 \text{ }\mu\text{m}$ ,  $\Delta r = 4 \text{ }\mu\text{m}$ , and  $\Delta \theta = B/500$  radians. Leibman's implicit formula [44] was used, since it has been shown to yield a stable solution independent of the time-step relative to the thermal time constant. Temperatures for the transient studies were obtained based on the Crank-Nicholson technique [45]. Isothermal conditions were assumed at all boundary surfaces, and their temperatures were set to the ambient value  $T_0$ . This effectively assumes that the GaAs system is capable of removing excess heat through radiation and convective processes. Equivalently, the assumed Dirichlet boundary conditions imply that the surfaces are sufficiently far away from the internal hot spots, and hence can be regarded as being in near-equilibrium with the ambient.

Our choice of the present method is based on considerations of computational ease and flexibility. For example, the finite element technique is complicated and cumbersome [46, 47], and is not needed for the relatively simple cylindrical geometry of the present problem. The transmission line matrix (TLM) for heat flow analysis has utility primarily in the time domain and for complex geometries [48, 49]. Since analysis over relatively long time scales is the present objective, use of the TLM would be inefficient. Finally, SPICE based circuit calculations based on the equivalence between thermal and the electrical systems [50, 51] require a large number of nodes, are not as transparent, and represent a "lumped-element" representation which are inappropriate for modeling high-frequency/ultrashort events.

## RESULTS AND DISCUSSION

Numerical simulations at room temperature were first carried out to obtain the internal temperature profile within the PCSS device in the presence of a current filament. As already mentioned, the treatment and analysis under filamentary conditions is important for two reasons. Filaments represent the least stable scenario for the PCSS. Hence, it is the worst-case situation that can be used to ascertain limits on the parameter space for thermally stable device operation. Second, for high power capability and increased switching efficiency, the device is typically used in the non-linear mode under which filamentary conduction is not unusual. The presence of a filament was taken into account by setting the generation function "g" to a

fixed value independent of time, with a spatially cylindrical distribution centered at the midpoint of the device. Thus, mathematically,  $g(r,z,t)$  was chosen as :

$$g(r,z,t) = k_0 [U(r)-U(r-r_1)] [U(z-z_1)-U(z-z_2)] , \quad (3)$$

where  $k_0$  is a constant thermal generation power density,  $U(z)$  is the Heaviside step function, while  $r_1$ ,  $z_1$  and  $z_2$  were fixed values in the range:  $0 < r_1 < R$ , and  $0 < z_1 < z_2 < L_z$ . Here  $R$  is the radius, and  $L_z$  represents the extent of the 2D simulation cylinder along the axial direction. Typical radii of the current filaments are on the order of 4  $\mu\text{m}$  as reported by et al. [9]. Filamentary current densities for the non-linear mode are at or above  $10^9 \text{ A/m}^2$  [52], while internal electric fields of  $5 \times 10^5 \text{ V/m}$  and higher have been reported [52]. This translates into a lower bound on the heat generation density parameter  $k_0$ , as given in equation (3), of  $5 \times 10^{14} \text{ Watts/m}^3$ . For realistic simulations, therefore, values of  $k_0$  close to this magnitude should be used.

Fig. 2 shows the simulation results of the internal steady state temperature profile for a 300 K ambient. The filament was chosen to be located at the center of the device having a radius of 4  $\mu\text{m}$ , with  $z_1 = 1 \text{ mm}$  and  $z_2 = 1.5 \text{ mm}$ . The total power dissipated within the filament was taken to be 1.2 Watt which translates into a local heat generation density  $k_0$  of  $4.77 \times 10^{13} \text{ W/m}^3$ . This is below the experimental report [52], and so one should expect thermally stable operation. The profile of Fig. 2 reveals a peak temperature of 340 Kelvin which is a relatively mild increase of 40 C. Nonetheless, the overall temperature profile is seen to be very non-uniform, and almost all of the heating takes place within the filamentary region. Next, the result at an increased heat generation density of  $1.2 \times 10^{14} \text{ Watts/m}^3$ , corresponding to a power dissipation of 3 Watts, is shown in Fig. 3. All other parameters and filamentary dimensions were kept unchanged. For this case, the peak temperature is predicted to be substantially higher at about 420 Kelvin. This increase clearly demonstrates that device self-heating, which is usually ignored in theoretical treatments of the PCSS, is an unrealistic assumption. The use of room-temperature transport and semiconductor parameters is also in serious error, and a careful reevaluation of these parameters as appropriate at these elevated temperatures needs to be made. Keeping the same power density, a subsequent simulation was carried out for a much longer 1.5 mm filament. The total power dissipation in this case had to be increased to 9 Watts (from the previous 3 Watts

value), due to the three-fold increase in the filamentary volume. Results shown in Fig. 4 reveal roughly the same peak temperature of about 420 Kelvin. This result demonstrates two points. First, it becomes evident that the *magnitude of the power density*, rather than the total power is critical in determining the internal temperatures. Second, a simple scaling rule for the total power with geometric volume is seen to hold.

The above steady state results are roughly in keeping with experimental trends. For example, thermally stable operation for an internal power density as high as  $1.2 \times 10^{14}$  Watts/m<sup>3</sup> has been shown to be possible here. This is on the same order of magnitude (though slightly on the lower side), as the experimental observation of stable PCSS behavior at  $5 \times 10^{14}$  Watts/m<sup>3</sup> [52]. Thermal simulations were next carried out for power densities beyond  $1.2 \times 10^{14}$  Watts/m<sup>3</sup> to determine whether a threshold limit for thermal stability may exist. A secondary objective was to determine if power levels closer to the experimental report could be attained with thermally stable behavior. The results of our simulations showed that for densities beyond  $1.3 \times 10^{14}$  Watts/m<sup>3</sup>, a stable solution did not result. A peak temperature of about 560 Kelvin was the highest that could be obtained from the simulations. This result can be reconciled by taking account of the fact that the experimental work was *not* conducted under dc conditions. Instead, the PCSS was repetitively switched into the high-current mode over finite durations, separated by "OFF" periods of low current levels. This means that the internal power dissipation was intermittent and that the devices were allowed to cool during the "off-cycle". Consequently, it is natural to expect that higher power densities would be sustained. This is consistent with the lower power density threshold predicted under dc conditions.

Simulations under transient conditions were carried out next to determine the extent to which the power dissipation density threshold could be extended. Fig. 5 shows the results of peak temperature at the device midpoint (at  $r = 0$ ), and a point located 10 microns off-axis, with and without temperature dependent thermal conductivity. A power density of  $2.3 \times 10^{16}$  Watts/m<sup>3</sup> was used for a 4 m radial filament of extent 1.5 mm. The generation was assumed to occur during a 50 ns period, followed by an OFF duration of 1 :s to yield a duty-cycle of about 0.05. The on-axis temperature in Fig. 5 for both cases, as expected, is substantially higher than at the off-axis spot. The interesting point is that unstable operation is predicted under these conditions when a temperature dependent thermal conductivity is used. The internal temperature does not reach a limiting, steady state value. Instead, over each 1.05 :s cycle, there is a continuous net increase in temperature, until a breakdown point is reached at about 4.2 :s. The thermal failure predicted here occurs for

an average power dissipation of :  $2.3 \times 10^{16} * 50 \times 10^{-9} / [1.05 \times 10^{-6}] = 1.09 \times 10^{15} \text{ Watts/m}^3$  . This average value is above the  $1.4 \times 10^{14} \text{ Watts/m}^3$  threshold obtained in the previous calculations, and hence in keeping with the predicted behavioral trend. However, when the simulation was carried out keeping the thermal conductivity constant at its room temperature value of  $46 \text{ Wm}^{-1}\text{K}^{-1}$  , the predicted results were quite different. Dramatically lower internal device temperatures are predicted for constant thermal conductivity. The peak, on-axis value, for example, is only 650 Kelvin and occurs at about 4.25 :s. The overall trend, though, is still a monotonic increase suggestive of thermally unstable behavior. The difference between the two sets of curves is quite large. It underscores the need to use proper temperature dependent thermal parameters for accurate analysis. Otherwise, heat conduction bottlenecks at the higher temperatures due to increased phonon-phonon scattering, would not be represented.

Reducing the density to  $4.6 \times 10^{15} \text{ Watts/m}^3$  with the same 50 ns ON time and a 1 :s OFF duration, produced the oscillatory curves for the midpoint and the  $r = 10 \text{ :m}$  off-center point, shown in Fig. 6. Even after 0.1 ms, a stable temperature is not seen, and an increasing temperature trend is predicted. The simulation was terminated after 0.1 ms for considerations of computational time. The average power density for this case, was  $4.6 \times 10^{15} * 50 \times 10^{-9} / [1.05 \times 10^{-6}] = 2.2 \times 10^{14} \text{ Watts/m}^3$  , which is above the  $1.3 \times 10^{14} \text{ Watts/m}^3$  threshold of the steady state simulations. A snapshot of the internal temperature profile at the 0.1 ms instant for this transient study, is shown in Fig. 7. The peak temperature is about 400 Kelvin, and occurs over the entire length of the 1.5 mm long filament situated along the z-axis. Finally, it must be mentioned that for a  $1.86 \times 10^{15} \text{ Watts/m}^3$  generation, a steady state with a peak temperature of 355 Kelvin was predicted. This value is below the predicted threshold, and hence consistent with the central results obtained here.

It is perhaps important to justify our use of a one-filament scenario in all of the present calculations. The basic notion of a power density threshold should hold under multi-filament conditions as well. However, it is qualitatively obvious that the single filament scenario considered here provides the worst case of device self-heating. If multiple filaments existed, but were sufficiently apart, there would be negligible mutual coupling, and the results given above should remain nearly unchanged. At small distances, however, the proximity effect could enhance the internal temperatures, if the current flowing through the individual channels was the

same as through a single filament. In practice, however, the current density at a given applied voltage, would not be the same in going from a multi-filament to a single filament situation. Instead, the current for an N-filament scenario has to be smaller by a factor  $1/N$  as compared to that of a single channel. This would naturally lead to a concomitant reduction in the power dissipation density as well. Consequently, despite mutual filamentary re-enforcements for the multiple filaments, the net contribution would not scale N-fold to produce the same temperature rise. The peak temperature values, for example, would actually decrease in going from a single filament to an N-channel scenario. Thus, a single filament represent the worst case, and so, the power density threshold obtained here provides a conservative guide for thermal stability predictions.

## CONCLUSIONS

Simulations were performed to determine the internal temperature profiles and peak temperatures of high-power SI-GaAs photoconductive switches. As is known from previous experimental work, device stability and operational reliability under repetitive conditions remain an issue. Filamentary currents that have been observed are thought to be responsible for device failures. Almost all previous studies on the PCSS, including analyses of potential breakdown under high power conditions have focused on carrier transport alone. Thermal aspects, and evaluations of a potential link between failure and the large power dissipation within localized filaments have not been examined. Here, a study was carried out to probe both the transient and steady-state thermal behavior of the PCSS under filamentary conditions. The approach was based on a time-domain, finite difference implementation of the heat diffusion equation taking account of the temperature dependent thermal conductivity.

The results obtained here suggest the existence of a threshold for safe and stable device operation based on considerations of internal heat generation. For single filament operation, which presents a worst scenario, no thermal instability is predicted below a power generation density level of about  $1.3 \times 10^{14}$  Watts/m<sup>3</sup>. This result is found to roughly hold under both dc and transient conditions. The prediction obtained here is in keeping with recent experimental data on PCSS devices, and produces a quantitative match with observations. Furthermore, it has been shown that even for densities below the threshold, substantial device heating can result. For example, a peak internal temperature of 560 Kelvin was predicted, which represents a 87 per cent increase from the room temperature ambient value. Hence, care must be exercised in incorporating temperature dependent parameters for self-consistent device simulations, even under stable

operating conditions. Finally, by extending the power density threshold idea, it can be argued that performance improvements and the ability to enhance the power/voltage-handling requirements for the PCSS are only possible by scaling the distance between contacts. Also, at best, only a linear improvement in the performance and stability with size can result. For example, the power density is crudely given by the product of the current (I) and voltage (V), and expressed as :  $P = V I / [L A] < P_{\text{threshold}}$  , where the cross sectional area is A, while L is the longitudinal length for current flow, and  $P_{\text{threshold}}$  the power limit for stability. Since the filamentary area is roughly fixed, the only possibility for enhancing the device power handling capability is to correspondingly increase the device length L. In practice, though, since the voltage will not be evenly distributed within the device, either due to multi-dimensional geometric effects or the presence of internal traps, only a sub-linear improvement with scaling can be expected.

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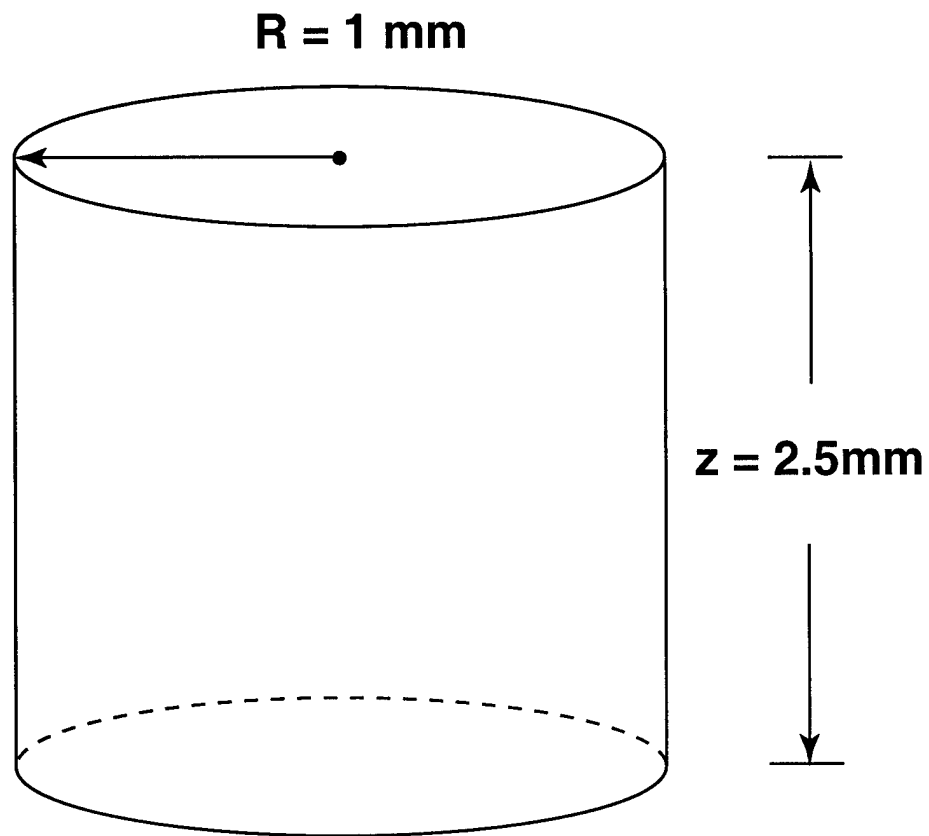


Fig. 1. Schematic of the PCSS switch geometry assumed for the simulations.

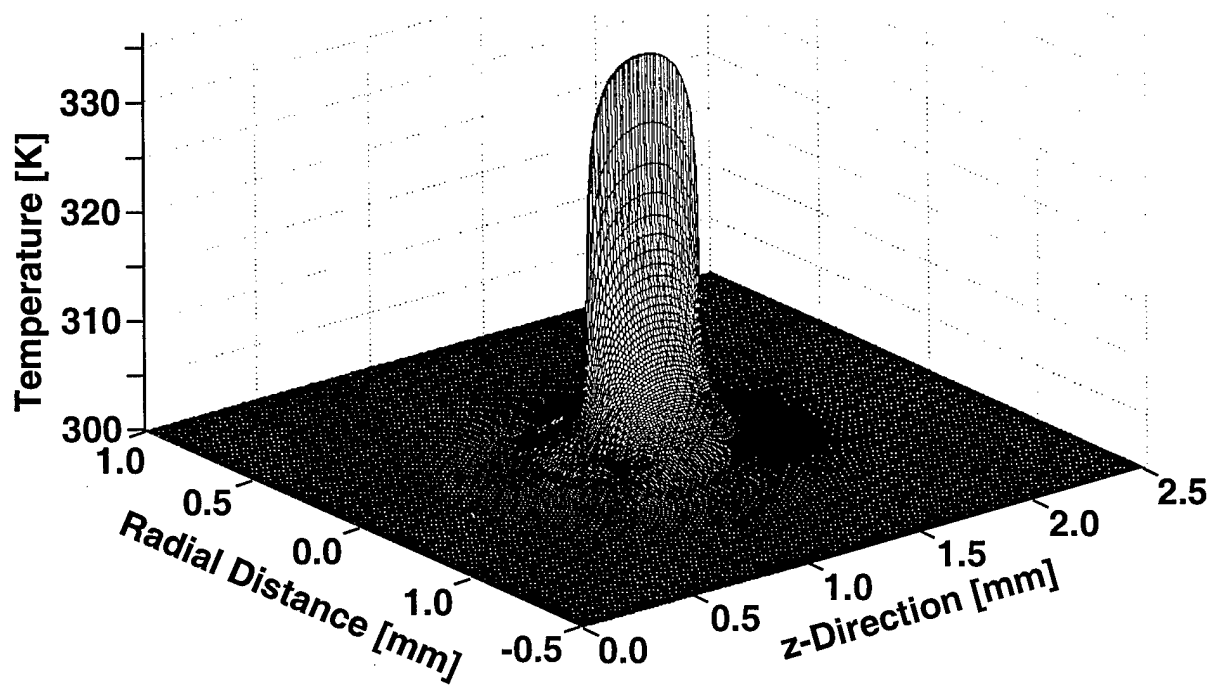


Fig. 2 Simulation results of the steady state internal temperature profile. A single 6 :m radius filament at the center was assumed with a power generation density of  $4.77 \times 10^{13}$  Watts/m<sup>3</sup>.

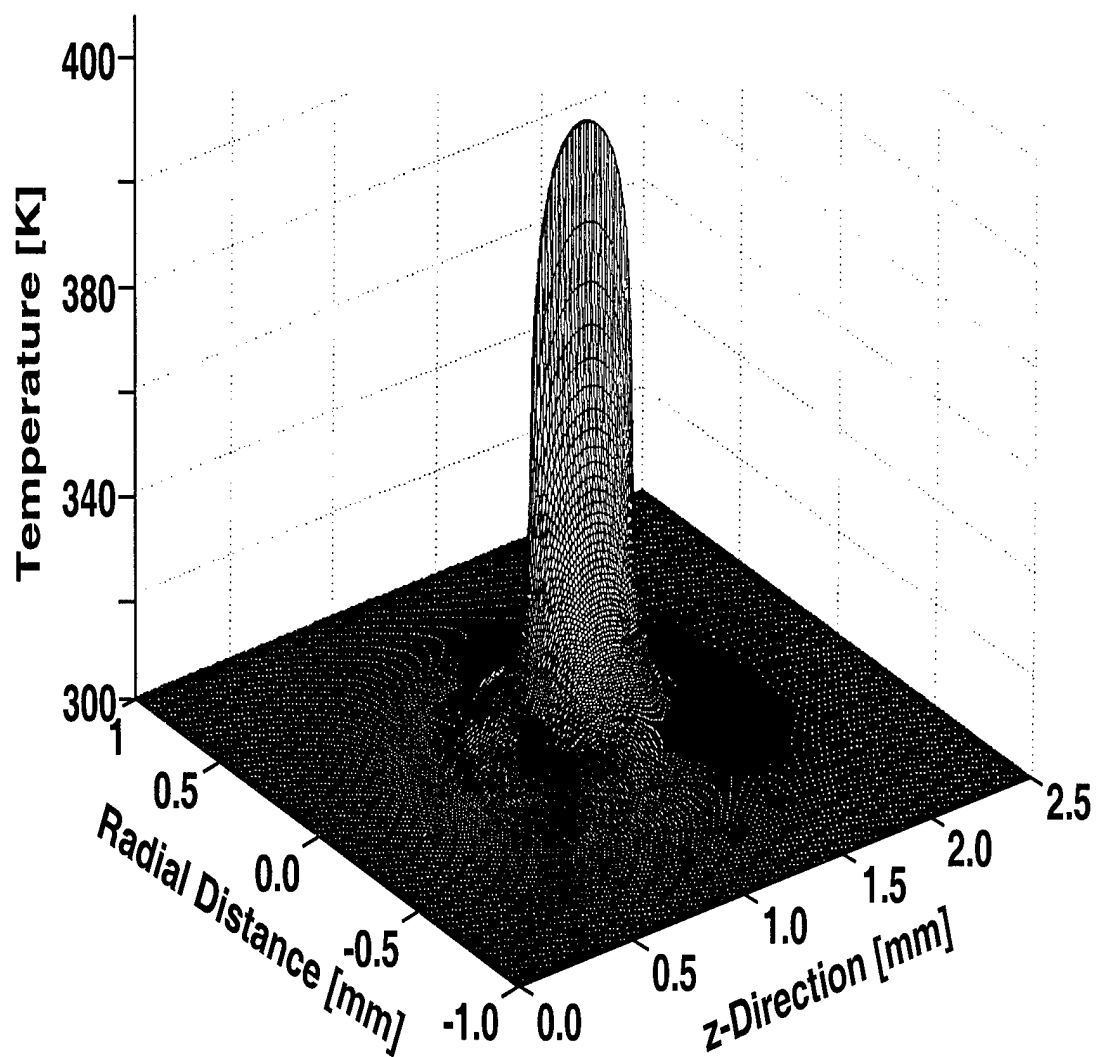


Fig. 3 Simulated steady state internal temperature profile for a generation power density of  $1.2 \times 10^{14}$  Watts/m<sup>3</sup> . All other parameters were the same as in Fig. 2.

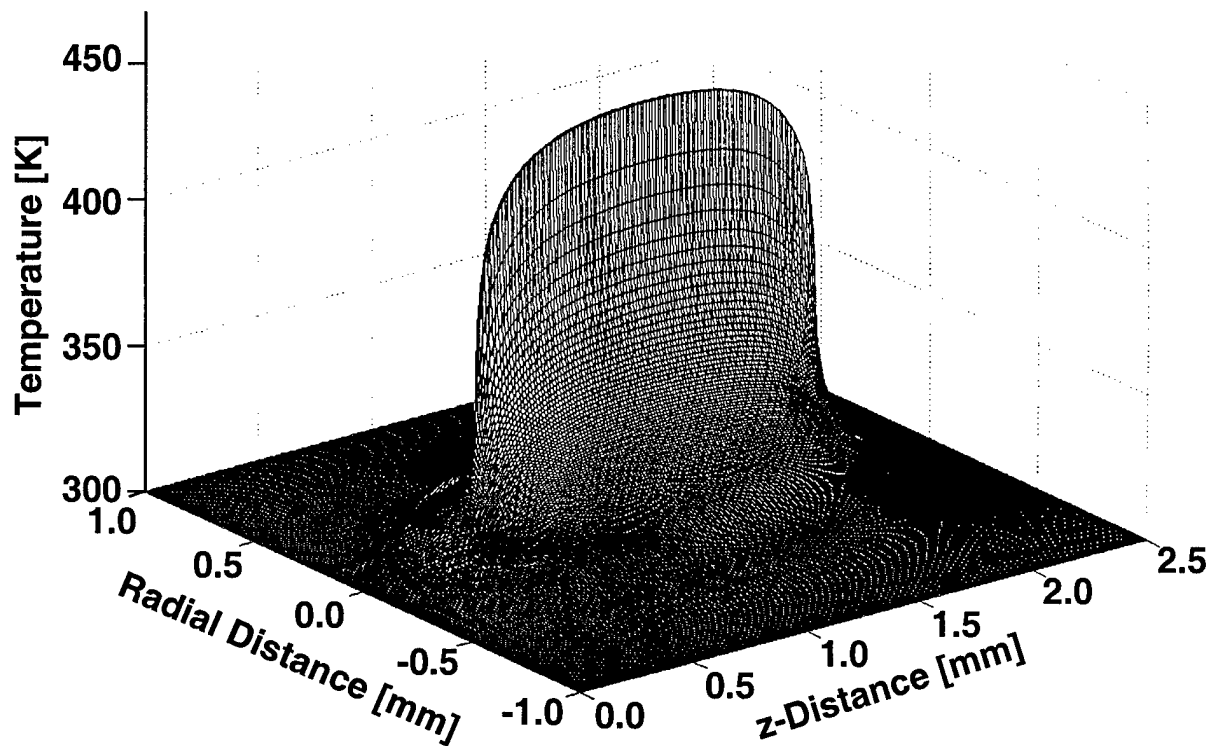


Fig. 4 Steady state results of the temperature profile for a generation power density of  $1.2 \times 10^{14}$  Watts/m<sup>3</sup> , but for a filament three times longer than considered in Fig. 3.

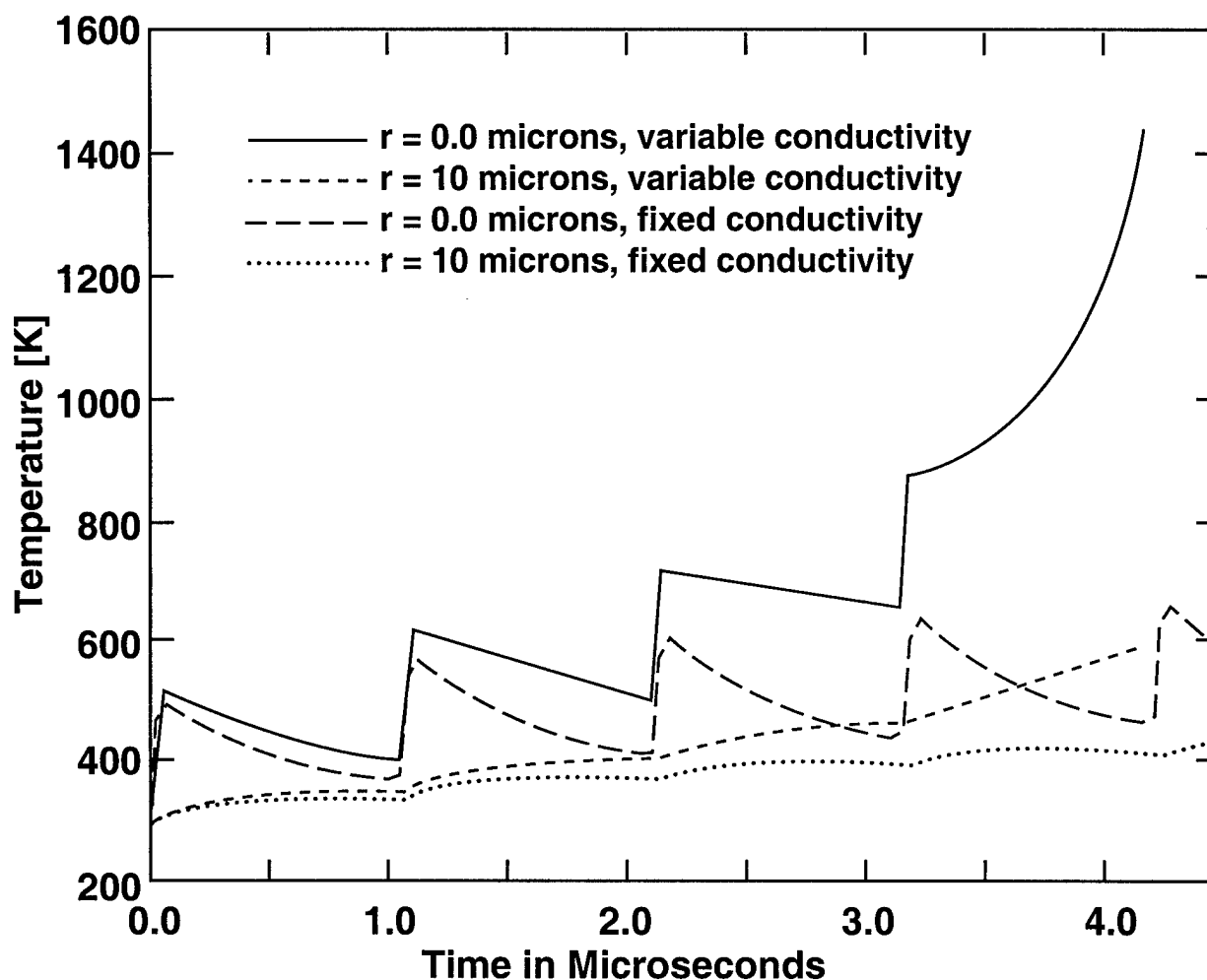


Fig. 5 Transient temperature results at two points within the PCSS. A  $2.3 \times 10^{16}$  Watts/m<sup>3</sup> power density was assumed with an ON time of 50 ns, followed by a 1  $\mu$ s OFF duration. Temperature dependent thermal conductivity, and a fixed conductivity of 46 Wm<sup>-1</sup>K<sup>-1</sup> were used.

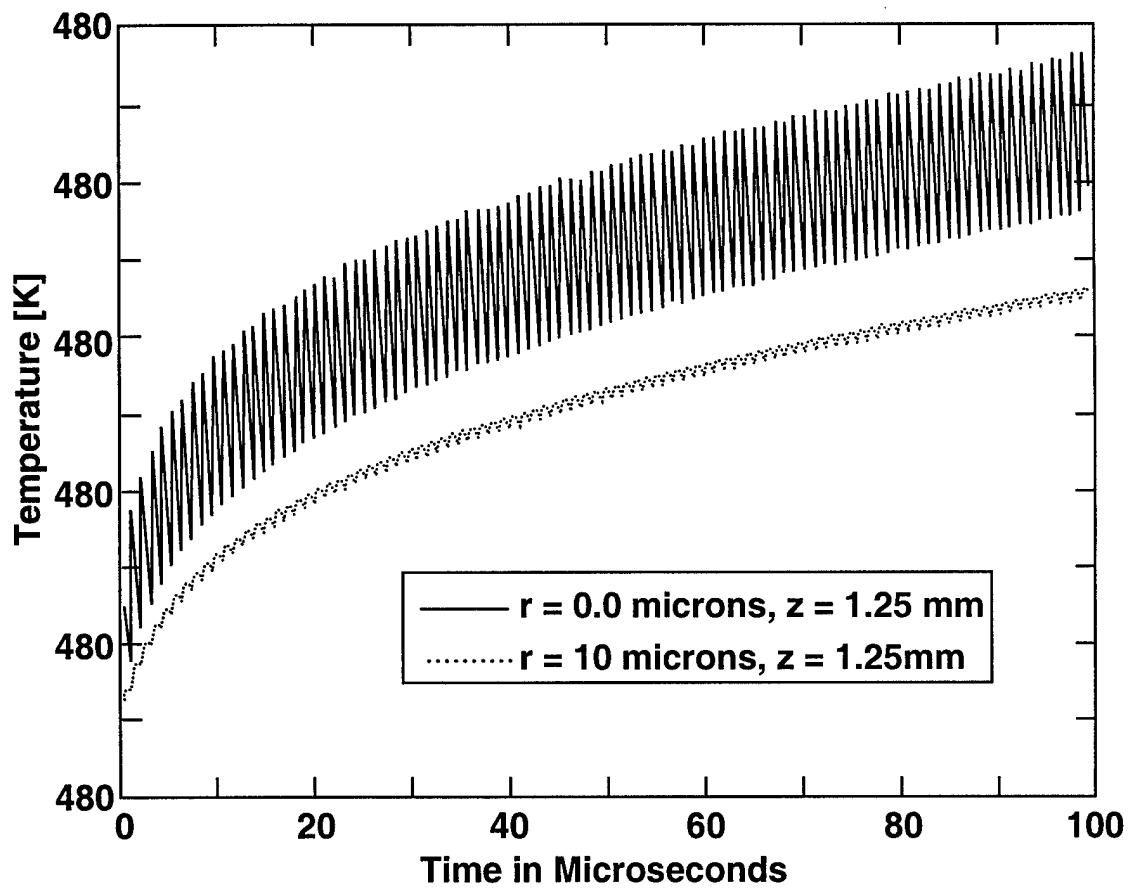


Fig. 6 Transient simulation results for a  $4.6 \times 10^{15}$  Watts/m<sup>3</sup> density over a longer time scale. The remaining parameters were the same as in Fig. 5.



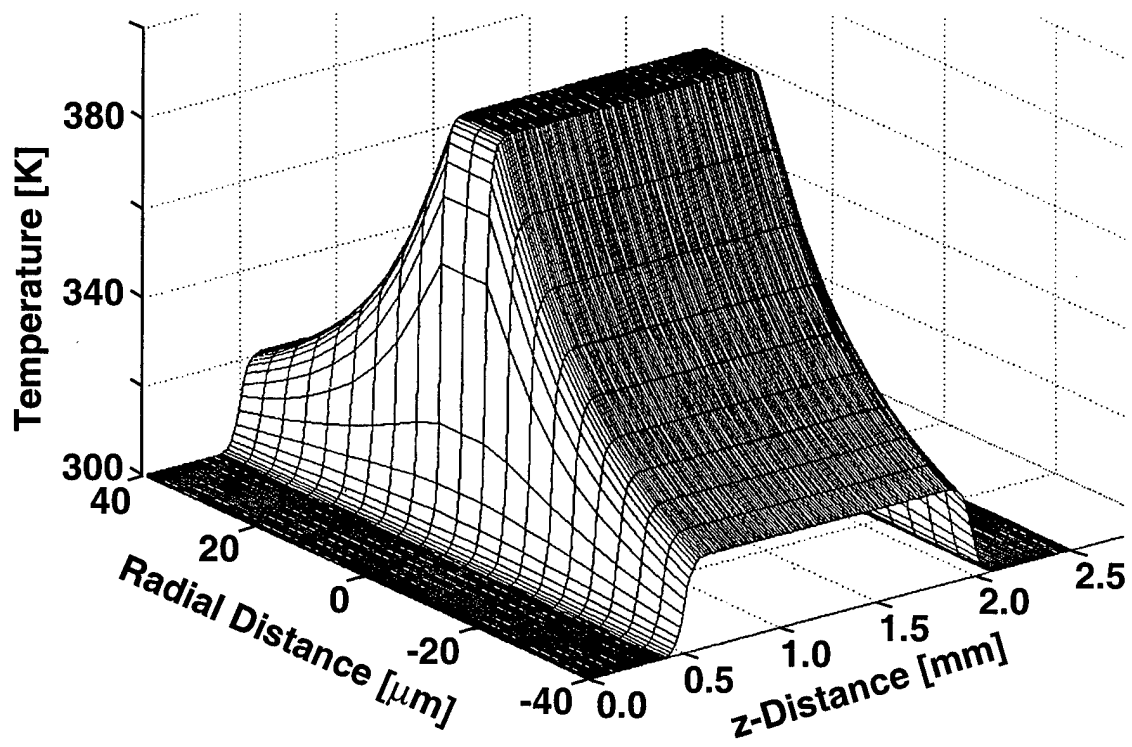


Fig. 7 A snapshot of the internal temperature profile at the 0.1 ms instant for this transient study of Fig. 6.

## APPENDIX G: IEEE Transaction on Nuclear Science (Published)

### ELECTRON IRRADIATION EFFECTS ON PHOTOCONDUCTIVE SEMICONDUCTOR SWITCHES (PCSSs) USED IN SUB-NANOSECOND TRANSIENT GENERATORS

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#### Abstract

Radiation-induced damage occurs in GaAs photoconductive semiconductor switches used in sub-nanosecond transient generators when subjected to 600 keV and 6 MeV electron irradiation. These switches are made from semi-insulating (SI) compensated material through a EL2/carbon compensation mechanism, and the liquid encapsulated Czochralski process. New defect levels are formed as a result of the non-ionizing energy loss (NIEL) process. The formation of new defect levels in the device alters the compensating balance between the existing deep level EL2 trap/donors and carbon acceptors, and changes the material properties. As a result, two important parameters of the device are adversely affected - the hold-off voltage of the switch at the pulse-charging (off) state, and the rise time during the conduction (on) state. The hold-off voltage shifts to a lower value since there are more trap-filled regions available that can fill up and alter the homogenous nature of the device material. Unstable filamentary conduction then occurs at a lower voltage and leads to premature breakdown. As with EL2 trap levels, new defect states induced by electron irradiation will further contribute to the delay in the rise time of the switch. The rise time determines the maximum energy transferred to the load.

The electron damage mechanism and its effects on the switch characteristics depend on the material properties. Intrinsic material or materials made through compensation other than through the deep donor and shallow acceptor balancing process are not expected to behave similarly. Simulation results at higher bias show a marked degradation of material properties. The switch current-voltage (I-V) characteristic when the bias increases to the kilovolt range is similar to trap-dominated semiconductors. An initial sub-linear current regime at low bias is followed by a super-linear regime of current flow at higher bias, and is in agreement with earlier observations.

#### I. INTRODUCTION

Photoconductive semiconductor switches (PCSSs) designed for high voltage applications are typically fabricated from intrinsic, low-doped, or compensated semiconductor material. Low jitter and low output impedance, and for some materials, smaller laser energy requirements in the "lock-on" mode are some of the advantages of these switcher. Since they require fast, repetitive switching action [1], gallium arsenide (GaAs) is the material preferred over silicon for this application. The switches typically have resistivity in excess of  $10^7 \Omega\text{-cm}$  and are usually made from the same material that is used as a substrate for active devices such as a MESFET. For SI GaAs material made through the liquid encapsulated Czochralski (LEC) process, the EL2 donor traps are compensated through carbon acceptors.

One application requiring high power is the generation of ultra-wideband (UWB) high power microwaves (HPM) [2]. Figure 1 shows the schematic of an UWB HPM generator and the PCSS used in the setup. The University of New Mexico and the AFRL at Kirtland AFB have set up a collaborative program for the fabrication, simulation study, and testing of the PCSS for HPM applications. The switches are also being tested in various radiation environments. Specifically, changes in the electrical and optical characteristics of the PCSS following electron irradiated are being studied. The switch dimensions are 2.0 cm by 1.3 cm with a thickness of

0.063 cm. The “opposed” contacts, made from layered Pd/Ge/Ti/Pt of thickness 200/400/400/300 Å, respectively, are on the front and back of the wafer, about 0.25 cm apart (Figure 1, inset). The Rogowski profile of the electrode and the opposed nature of the contacts help in improving the hold-off voltage and the rise time of the output pulse [2]. The rise time determines the maximum energy transferred to the load during switching action.

The switching process of the PCSS is a three-phase operation [3] that involves i) an initiation phase that occurs before the fast increase in photocurrent, ii) the sustaining phase, and iii) the recovery phase. A delay in the initiation phase may result in an overall increase in the rise time of the device [4-6], and thus may affect its performance. The origin of the delay time depends on the switch material and its properties, specifically those related to the trap sites and surface conditions that influence reflection and transmission of the incident photons [6]. The switches are also prone to premature breakdown that may be attributed to unstable filamentary conduction due to trap-filled regions that are formed at higher bias. Thus it is of interest to know how a radiation environment affects the switch rise time and early breakdown characteristics.

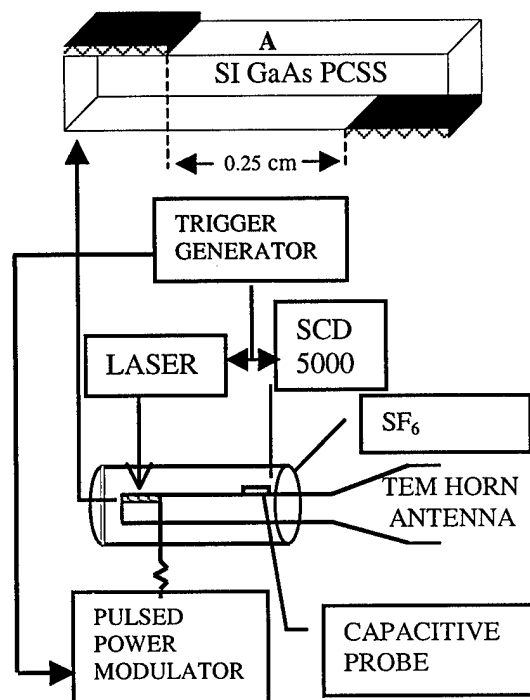


Figure 1: Sub-nanosecond radiation source setup and an enlarged view of the opposed contact PCSS (top).

Radiation damage due to the interaction of the PCSS with electrons, protons, neutrons, single charged particles, and gamma rays [7] will affect the device’s material characteristics and the performance of the pulse generator. Since GaAs solar cells are known to degrade through electron damage [8], it is of interest to see how materials made through the compensated process involving a high density of traps would behave during a radiation transient.

In this paper, we present experimental results and the analysis of PCSS material degradation following electron irradiation at two different electron energies. The devices were subjected to electron dosages with energies ranging from the keV to MeV range. We also present simulation results that will provide insight into the physical conditions within the device such that meaningful measures to minimize damage can be incorporated in the system.

## II. EXPERIMENTAL SETUP

Photoconductive switches made by Bertram Laboratories and the University of New Mexico were exposed to 600 keV and 6 MeV electrons using facilities at the AFRL/Phillips Site and the Health Sciences Center of the University of New Mexico.

### A. Electron Irradiation

The experimental setup for the low energy experiment is shown in Figure 2. The radiation source, manufactured by Radiation Dynamics Inc. (RDI), is a 1 MeV-electron accelerator with a maximum current output of 400 mA. The beam diameter at the output window of the accelerator is approximately 0.635 cm. For this experiment, the beam was scanned along both the X and Y-axes at a repetition rate of 427 and 396 Hz. The beam energy was 600 keV at a current of 100  $\mu$ A and the window of the scan was 2.54 x 2.54 cm, which resulted in a flux of about  $1 \times 10^{14}$  electrons/cm<sup>2</sup>-sec for this experiment. The electron beam in all the experiments was incident onto the anode side of the device (marked A in Figure 1). This is also the region where the laser beam is incident during the on state of the switch.

Our initial analysis suggests that a high level of trap occupancy at any junction leads to breakdown [9] since a change in the device characteristics leads to unstable current filamentation. Radiation damage therefore is expected to affect not only the hold-off characteristic of the device, but also its rise time, as stated earlier

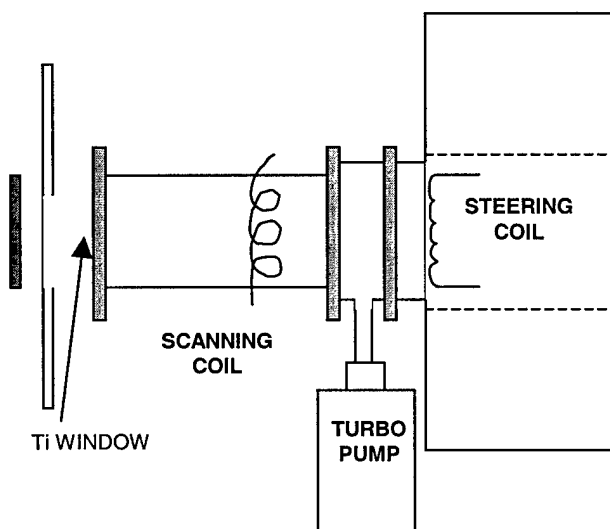


Figure 2: Experimental setup for 600 keV electron irradiation of the PCSS.

For premature breakdown, it is not essential that damage be confined to the bulk of the device; defects at the surface or at any depth may affect the device's performance. Initial calculations (to be described later) suggest significant penetration of the electron beam, even for the 600 keV source.

The irradiation of the devices at high electron energies was performed at the University of New Mexico Cancer Research Center. The irradiator was a Varian Clinac 2500 linear accelerator that was utilized in the electron mode for this experiment. Exposures were at a distance of 60 cm from the beam output and each exposure was at 200 Gy, determined through TLD and Faraday cup measurements. Each exposure was set for 2.42 minutes with a total of 45 exposures, yielding a total dose of about 9,000 Gy. The beam energy was 6 MeV, but upon passing through a medium to scatter the beam to cover a larger area the end point energy at device level was 4 MeV. The devices were placed on a sheet of plexiglass 60 cm from the beam output. Measurements were taken approximately one hour after irradiation.

## B. Measurement Technique

The devices were evaluated using a HP-4142 Parametric Analyzer. This instrument was selected for the short pulse duration of voltage that was applied to the test devices during the measurement process. The unit used for the measurement was a HP41423A, High Voltage Source/Monitor Unit (HVSMU) that has a range of 2 mV to 1,000 V and can supply a current from 2 pA to 10 mA. During the measurements the devices were placed in a test head that was covered for maximum assurance that no light was incident upon the device. The HVSMU was configured to operate in the "Constant Pulse" mode for each measurement using a pulse duration of 400 ms.

When each device was evaluated there were 5 different pulses applied and measured: 200 V, 400 V, 600 V, 800 V and 1000 V. The measurements had a 3-minute period of wait time [no voltage] before the next test pulse was applied. This was to ensure that the device would not be saturated before the next measurement. During each measurement, both voltage and current were measured on the device. The HVSMU was connected to one terminal of the device and the other terminal was connected to the system ground. To ensure repeatability of the measurements, the devices were measured three times. All the data to be presented are therefore the average value for three repeats. On one of the devices the measurement at 1,000 V was not repeated.

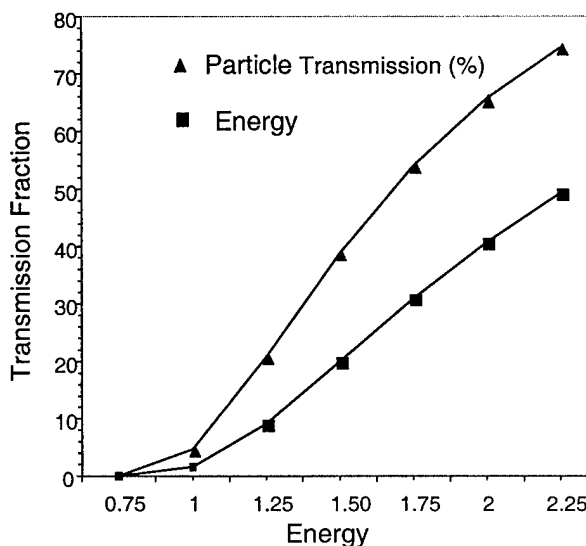


Figure 3: Transmission of 600 keV electrons through the 630  $\mu\text{m}$ , semi-insulating GaAs PCSS.

Prior to irradiation, simulations were performed using the CEPX/ONELD code [10] to ensure electron penetration into the device. Figure 3 shows the results for the low energy electrons. At 0.75 MeV the particle transmission is 0.01% and at 1 MeV it is 4.7% while the energies transmitted are 0.02% and 1.59%, respectively. Since these values are at the cathode side of the wafer (electrons are incident onto the anode side), it suggests sufficient transmission of particles in the 0.063 cm GaAs layer. A density value of 5.82  $\text{g/cm}^3$  and weight compositions of 0.4820% for Gallium and 0.518% for Arsenide were taken for these calculations.

## C. Results

Figure 4 shows the I-V plot for a PCSS irradiated at the AFRL facility. The calculated dose was 121 Mrad (Si) with a Faraday cup reading of 14.34  $\mu\text{A}$  for an exposure time of 4.53 min for each irradiation step.

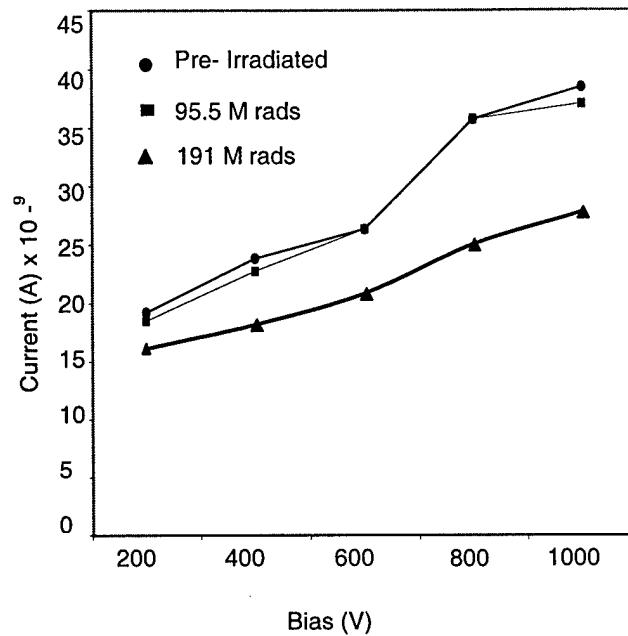


Figure 4: Response of the PCSS prior to irradiation and at two dose levels with 600 keV electrons.

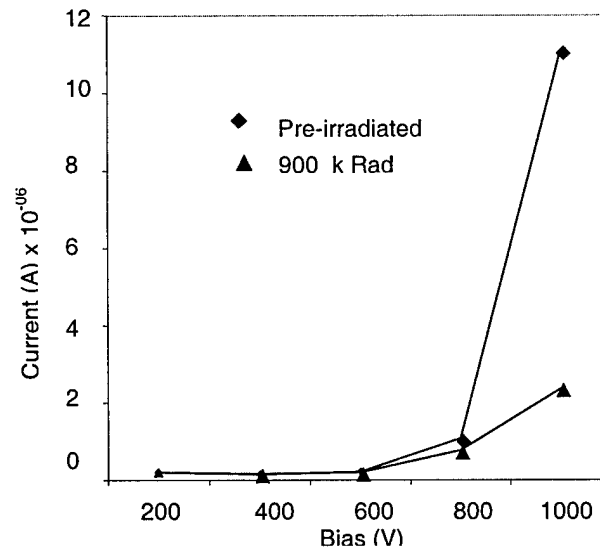


Figure 5: The I-V characteristic of the switch before and after exposure to 4 MeV electrons using the UNM accelerator.

There is no substantial change in the device material characteristics after the first dose step, but degradation is apparent at subsequent doses. The I-V characteristics of a sample switch following irradiation at 6 MeV (4 MeV at the device) at the UNM facility is shown in Figure 5. As can be seen there is an initial slow increase in current, followed by a sudden shift at around 600 V.

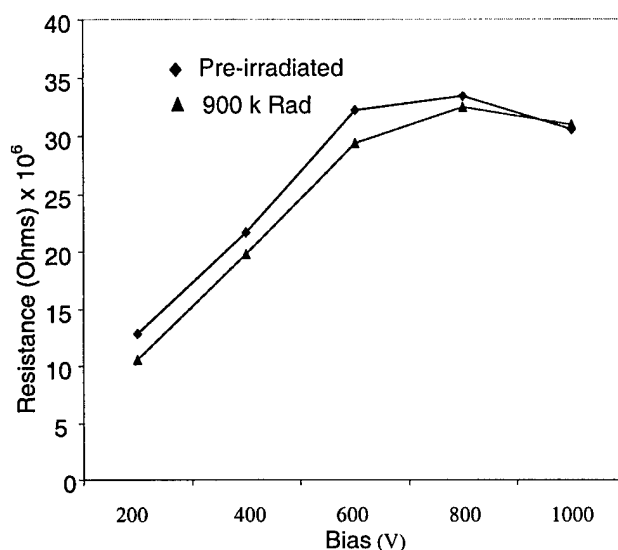


Figure 6: Resistivity of a PCSS before and after exposure to energetic electrons.

The plots are similar for both the irradiated and un-irradiated samples. Degradation of the current values at high bias is evident for the exposed sample. The resistivity change for another switch is shown in Figure 6. Some fluctuations in between samples were found. Switches (not shown here) that had extreme fluctuations in their characteristics both before and after irradiation were discarded. The figures shown here are typical representative samples (switches showing similar characteristics) of a batch of three, tested both for low and high-energy electron irradiation. Due to high cost it was not possible to test a larger sample.

### III. SIMULATION MESH

Simulations were carried out using the SILVACO International software for semiconductor studies [11]. This is a comprehensive tool that unites semiconductor process, device and circuit simulations, and includes numerous models and parameters. In a "mixed-mode" environment the device can be placed in a circuit and the effects of any changes in the device parameters on the overall circuit can be studied. In addition to the drift-diffusion model one can use the energy balance model to study such "non-local" effects as velocity overshoot, reduced energy dependent impact ionization, etc. In this case mobility and impact ionization become functions of the local carrier temperature rather than the local electrical field. Finally, the code also has provisions to incorporate user-defined functions and parameters through an interactive C-interpreter. Besides known models, effects such as surface roughness, phonon scattering, and interaction between carriers and ions in the vicinity were also incorporated in the input. Some other parameters include field enhanced tunneling, effective contact resistivity, and parameters for subsurface conduction [13].

Table I

Device Parameters.

Distance between contacts	0.25 cm
Contact length	100 $\mu\text{m}$
Carbon doping	$3 \times 10^{15} \text{ atoms / cm}^3$
EL2 trap level	0.730 eV
Electron capture x-sections	$4 \times 10^{-16} \text{ cm}^2$
Hole capture x-sections	$2 \times 10^{-18} \text{ cm}^2$

Table I summarizes the device parameters used in the simulations. Details are provided elsewhere [9,12].

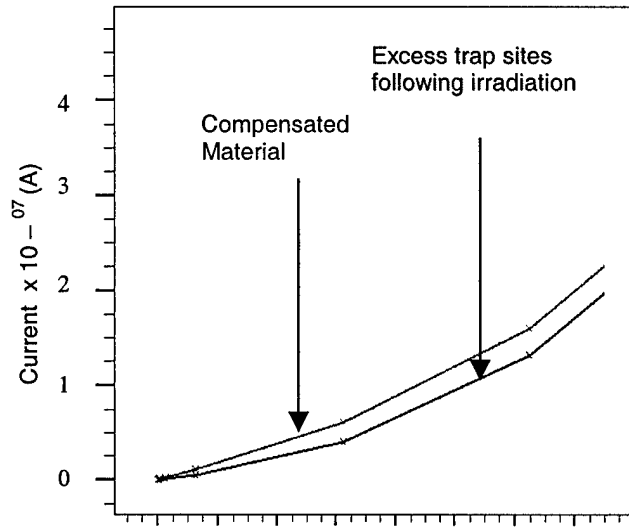


Figure 7: Plot showing the response of the PCSS before and after irradiation, resulting in parameter degradation.

The incorporation of this model shows a better correspondence between the experimental and simulation results, specifically in predicting the devices' I-V characteristics and breakdown voltage [9].

In the simulations it was assumed that, as a result of electron-device interaction and the subsequent damage to the device, new defect site at the mid-gap are created. Thus the effective capture cross section of the carriers are altered. This changes the carrier lifetime and the trapping and de-trapping effects associated with the site. In Figure 7 the I-V characteristic is similar to the device at low electron energy irradiation. The difference in current values may be attributed to i) the difference in the dimensions of the simulation mesh and the actual device and, ii) arbitrary value for carrier capture cross section. Figure 8 shows the simulated I-V for the pre- and post-irradiated devices. It shows the initial slow increase in current, followed by a much faster rise, which is typical for trap-dominated semiconductors [14]. At high fields electrons gain enough energy to reach the cathode and the double injection phenomenon leads to a sudden increase in current [15]. The plots also show the change in the conductivity as a result of increased trap sites that effectively dominate the device performance at high power operation [9].



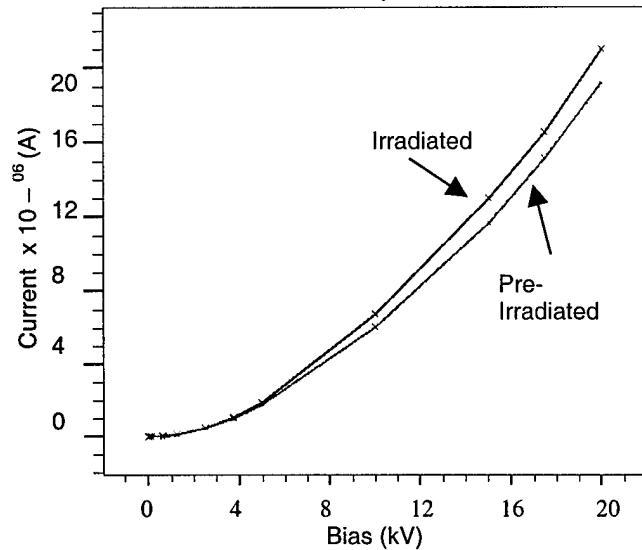


Figure 8: I-V characteristics showing an initial slow increase in current followed by a fast rise with changing bias

Figure 9 shows the rise time of the switches during the conduction (on) state. Both plots are for the case when the switch is charged to 20 kV. A laser beam of wavelength equivalent to the band-gap energy was incident onto the anode side of the switch. The laser was incident along the surface except for 100  $\mu\text{m}$  at the edges. This was done in order to avoid interactions with the contact materials.

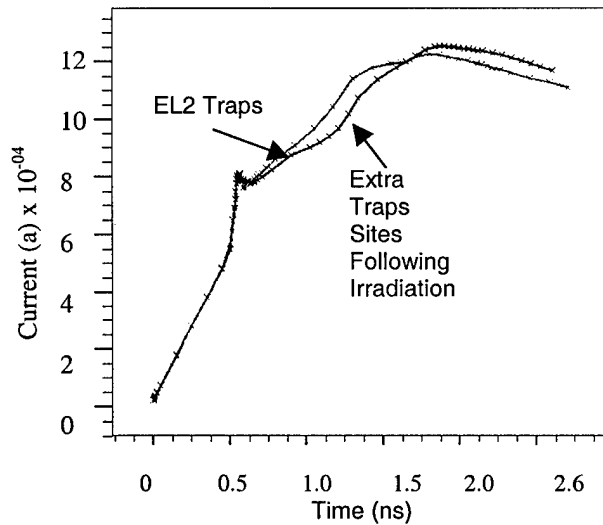


Figure 9: Initial response of EL2/carbon compensated PCSS and with excess traps generated following electron irradiation [16,17].

#### IV. DISCUSSION AND CONCLUSION

Even though compensated SI GaAs is designed to act as a non-conducting medium at low bias conditions, during high power operation and under radiation transients its current carrying properties changes

drastically. Prior to irradiation, the presence of the EL2 trap sites near the mid-gap basically controls the electrical properties of the PCSS. The conduction mechanism is similar to that of Fe doped InP, where there is a drastic change in the material properties due to a mid-gap energy level as a result of Fe doping [18]. The I-V characteristics can be explained as follows: since there is a difference in the electron and hole capture cross-section values for EL2 level, it acts as a trap rather than a recombination center. Injected electrons are thereby captured, leading to an increase in the hole lifetime. Thus, initial conduction is through single injection. At high fields de-trapping occurs and released electrons have sufficient energy to reach the anode and also generate carriers due to impact ionization [15]. Therefore, we see a sudden increase in current, as shown in Figures 5 and 8.

Following irradiation, more trap sites are created as is evident from the experimental results. The material conduction properties would change further and affect the filamentary nature of conduction, which is characteristic of the switches. Unstable filamentary conduction and surface flashover are both affected by defect sites [9, 15]. The PCSS response will then depend on the excess trap concentration, capture cross-section, field dependent trapping and de-trapping effects, etc.

Since the rise time delay is associated with trap filling at deep levels in the PCSS [5], similar effects are expected for the switches following electron irradiation. However, if de-trapping occurs at a much lower field than before an increase in the initial current will improve the rise time. Delayed de-trapping has the opposite effect on the rise time. As is evident from Figure. 5, there is a substantial reduction in de-trapping when irradiated with 4 MeV electrons.

The effects of the traps on the premature breakdown mechanism are more complex. Material resistivity (and hold-off) may increase due to the trap levels introduced. Our simulation results show de-trapping at a faster rate for the irradiated sample at high voltage during the off state (Figure 8) and also during the on state after about a nanosecond (Figure 9). Electrons trapped for a long time period as compared to the switching frequency also affect the device performance. This may lead to premature breakdown due to unstable filamentation and charge accumulation.

In summary, rise time and premature breakdown are two parameters that affect the performance of the PCSS. These important switch parameters affect the device performance, specifically at high bias conditions while generating ultra-wideband high power microwaves. Depending on the nature of the compensation mechanism (or the trap levels already present in the material), electron irradiation and the addition of defect sites affect both of these parameters and subsequently the performance of the switches. Since these defects in a trap- dominated device material is being reported for the first time, further studies to characterize these defect sites (concentration, energy, and cross sections) are necessary in order to ensure meaningful simulation results such that expensive repeat experiments can be avoided.

### ACKNOWLEDGMENTS

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